

## Arithmetic Logic Unit

### Object

To investigate the properties of an arithmetic logic unit (ALU) and to use it to evaluate simple arithmetic expressions.

### Parts

- (1) 7404 Hex Inverter
- (2) 7476 Dual J-K Flip-flop
- (1) 74181 ALU/Function Generator

### Study sections

*Computer Systems*, Fourth Edition, Jones and Bartlett Publishers: Section 10.4, Combinational Devices; Section 12.1, Constructing a Level-ISA3 Machine.

### General information

An arithmetic logic unit (ALU) is a basic unit in computers. As the name implies, it performs various arithmetic and logical operations on the inputs (operands). The operation performed depends upon how the function select lines are set.

The five function select inputs of the 74181 ALU consist of one mode control (M), and four select inputs (S3, S2, S1, S0). When M = 1, logic functions are realized. When M = 0, arithmetic functions are realized. The arithmetic functions also use the carry-in.

The listing of available functions and the encoding is in the parts list. You will use the table for ACTIVE HIGH DATA. High voltage represents 1, and low voltage represents 0. Notice that with this table the carry in Cin (denoted Cn in the spec sheet) and carry out Cout (denoted Cn+4) in the spec sheet) are asserted low. That is, Cin = 1 means no carry, while Cin = 0 means a carry has occurred. In the table "+" means logical OR, and "PLUS" means addition. Note that some logical operations are possible when the arithmetic functions are realized.

### Procedure

#### 1. Logic Functions

Calculate the 16 values of F for A = 1010 and B = 1001 by referring to the table in the specification sheet for the 74181 ALU assuming the mode input M is high. Enter them into the "F Predicted" column of the table in Figure 1.

Construct the circuit shown in Figure 2. Connect M = 1 and Cin = 1. Select the functions with the switches and enter the values of F in the column labeled "F Observed" by reading the logic indicator LEDs.

How does the Observed column compare with the Predicted column? \_\_\_\_\_

**Figure 1**

A = 1010, B = 1001, M = 1

S3 S2 S1 S0 SW1 SW2 SW3 SW4	Function	F Predicted F3 F2 F1 F0 LE LF LG LH				F Observed F3 F2 F1 F0 LE LF LG LH			
0 0 0 0									
0 0 0 1									
0 0 1 0									
0 0 1 1									
0 1 0 0									
0 1 0 1									
0 1 1 0									
0 1 1 1									
1 0 0 0									
1 0 0 1									
1 0 1 0									
1 0 1 1									
1 1 0 0									
1 1 0 1									
1 1 1 0									
1 1 1 1									

Instructor verification: \_\_\_\_\_

[illegible]

Connect M = 0, and maintain Cin = +5V (no carry). Calculate the 16 values of F for A = 1010 and B = 1001 by referring to the table in the specification sheet for the 74181 ALU assuming the mode input M is high. Enter them into the “F Predicted” column of the table in Figure 3.

How does the Observed column compare with the Predicted column? \_\_\_\_\_

**Figure 3**

A = 1010, B = 1001, M = 0, Cin = 1 (no carry)

S3 S2 S1 S0 SW1 SW2 SW3 SW4	Function	F Predicted F3 F2 F1 F0 LE LF LG LH				F Observed F3 F2 F1 F0 LE LF LG LH			
0 0 0 0									
0 0 0 1									
0 0 1 0									
0 0 1 1									
0 1 0 0									
0 1 0 1									
0 1 1 0									
0 1 1 1									
1 0 0 0									
1 0 0 1									
1 0 1 0									
1 0 1 1									
1 1 0 0									
1 1 0 1									
1 1 1 0									
1 1 1 1									

### 3. Evaluating multiplications

A series of operations could be performed if we had a register to store the ALU output and then used this data in the next operation. A register of this type is called an accumulator. Operations are performed on the accumulator and the input data and stored back in the accumulator.

For example, a multiplication could be performed by repeatedly adding the input register to the accumulator. The partial sum, however, must not exceed the maximum value representable by the ALU or the accumulator.

Construct the circuit shown in Figure 4. Clear the accumulator with switch Y.

To multiply  $3 \times 4$  enter 3 (0011) in switches SW5 through SW8. Then select the addition function  $F = A + B$  by setting switches SW1 through SW4 to 1001. The multiply by 4 is now accomplished by clocking with switch X four times (adding  $3 + 3 + 3 + 3$ ).

Does your circuit give  $F = 12$ ? \_\_\_\_\_

The last clock pulse from switch X simply loads the ALU output into the accumulator. The value Cout of the ALU that corresponds to the displayed value on lights LE LF LG LF is displayed by light LD just before the last clock pulse. The first entry of Figure 5 shows the result.

Multiply  $4 \times 4$  using the same procedure and check the value of Cout on the penultimate clock pulse. Record your results in the second row of Figure 5.

Perform the additional multiplications and list the results in the table of Figure 5.

[illegible]

		<u>+5V</u>	<u>Gnd</u>
<u>I</u>	7404	14	7
IC1, IC2	7476	5	13
ALU	74181	24	12

**Figure 5**

A	Number of switch X clock pulses	Result after the last switch X clock pulse	Count after the <i>penultimate</i> clock pulse	“Carry” or “No Carry”?
3 (0011)	4	12 (1100)	1	No carry
4 (0100)	4			
4 (0100)	3			
2 (0010)	7			
2 (0010)	8			

To evaluate expressions involving more than one type of operation or different input values, change the switches for A while the accumulator retains the partially evaluated expression. For example, to evaluate  $F = 3 + 2$ , perform the following two steps:

	ALU function					Result			
A	S3	S2	S1	S0	Description	LE	LF	LG	LH
	SW1	SW2	SW3	SW4					
3 (0011)	0	0	0	0	Sets F to 3	0	0	1	1
2 (0010)	1	0	0	1	Accumulates $F = 3 + 2$	0	1	0	1

In The following table, list the sequence of switch settings you must do to perform  $F = 4 \times 3 + 2$ . Perform the multiplication by accumulating 3 four times. Verify the sequence with your circuit.

A	ALU function S3 S2 S1 S0 SW1 SW2 SW3 SW4	Description	Result LE LF LG LH



In the following table, list the sequence of switch settings you must do to perform  $F = -(4 + 3)$ . You must perform the addition first, then negate. Hint: Consider the 0110 function of the ALU to do your negation in one step. Verify the sequence with your circuit.

A	ALU function	Description	Result
	S3 S2 S1 S0		LE LF LG LH
	SW1 SW2 SW3 SW4		

Instructor verification \_\_\_\_\_