Digital Circuits Labs
J. Stanley Warford

This is the parts list for a set of six digital circuit labs for use in conjunction with the textbook *Computer Systems*, Jones and Bartlett Learning. The labs refer to the fourth edition, but the references apply to the fifth edition as well. The labs and circuit designs are based on those from a UCLA undergraduate course I took in the late 1970's. I have modified the circuits and lab questions based on use with my own students over the years. Unfortunately, an exact attribution of the original labs is currently not possible, but I believe the original designs were due to Professors Bussel, Kinney, and/or Tseng.

The switch and lamp labels correspond to those of the Digital/Analog Trainer Model XK-550 manufactured by Elenco Electronics, Inc. However, it possible to use any generic breadboard kit of the instructor's choosing.

Lab 1, Basic Logic Gates
Lab 2, Combinational Logic Circuits
Lab 3, Sequential Circuits: Flip-flops and Shift Registers
Lab 4, A Combinational-Sequential System
Lab 5, Variable Modulus Decade Counter With Display
Lab 6, Arithmetic Logic Unit

Qty	Part number	Description
1	7400	Quad 2-Input NAND Gate
1	7402	Quad 2-Input NOR Gate
1	7404	Hex Inverter
1	7408	Quad 2-Input AND Gate
1	7432	Quad 2-Input OR Gate
1	7447	BCD to 7-Segment Decoder/Driver
2	7476	Dual Master-Slave J-K Filp-Flop with Clear and Preset
2	7485	4-Bit Magnitude Comparator
2	7486	Quad 2-Input XOR Gate
1	74151	8-Input Multiplexer
1	74164	8-Bit Serial In/Parallel Out Shift Register
1	74176	4-Bit BCD Decade Counter
1	74177	4-Bit Binary Counter
1	74181	4-Bit Arithmetic Logic Unit (ALU)
1	MAN71A	Common Anode 7-Segment Display

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

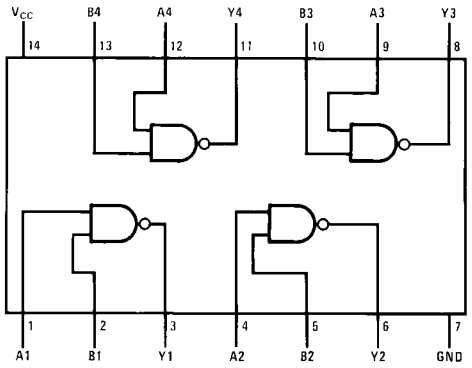
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

FAIRCHILD SEMICONDUCTOR TM

March 1998

DM7402
Quad 2-Input NOR Gates

General Description

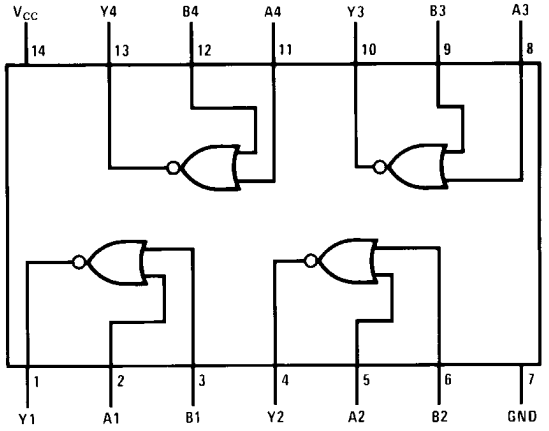
This device contains four independent gates each of which performs the logic NOR function.

Features

- Alternate Military/Areospace device (5402) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5402DMQB, 5402FMQB, DM5402J, DM5402W or DM7402N
See Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

FAIRCHILD SEMICONDUCTOR TM

March 1998

DM7404
Hex Inverting Gates

General Description

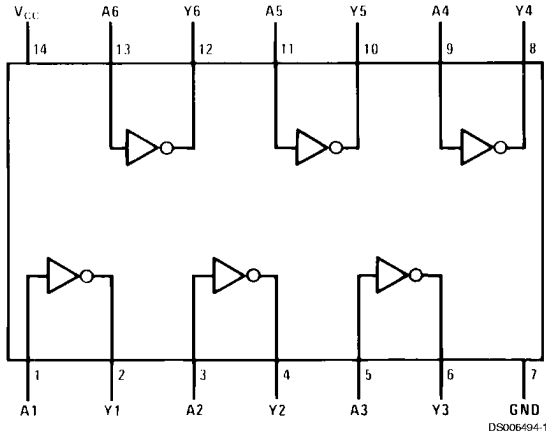
This device contains six independent gates each of which performs the logic INVERT function.

Features

- Alternate Military/Aerospace device (5404) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5404DMQB, 5404FMQB, DM5404J, DM5404W, DM7404M or DM7404N
See Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A}$$

Inputs	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

FAIRCHILD SEMICONDUCTOR TM

March 1998

DM7408
Quad 2-Input AND Gates

General Description

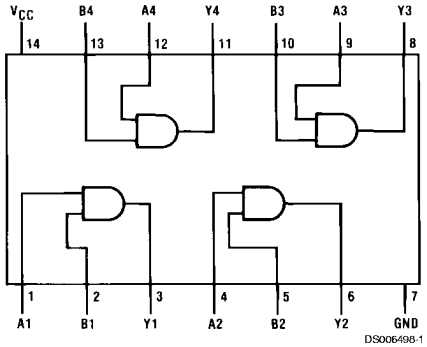
This device contains four independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (5408) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5408DMQB, 5408FMQB, DM5408J, DM5408W or DM7408N
See Package Number J14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

FAIRCHILD SEMICONDUCTOR™

June 1986
Revised March 2000

DM74LS32
Quad 2-Input OR Gate

General Description

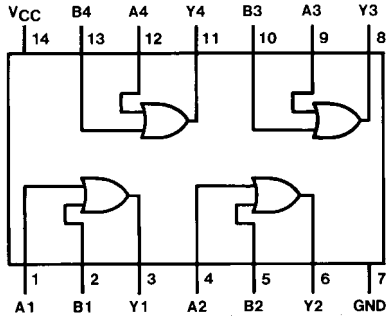
This device contains four independent gates each of which performs the logic OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS32N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

FAIRCHILD SEMICONDUCTOR™

October 1988
Revised March 2000

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 μA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

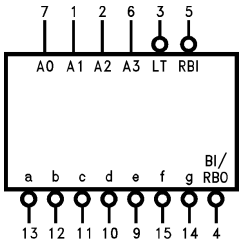
- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Ordering Code:

Order Number	Package Number	Package Description
DM74LS47M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS47N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

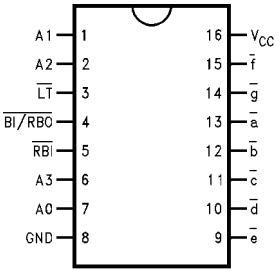
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$ –$\overline{g}$	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

Note 2: $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 3: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

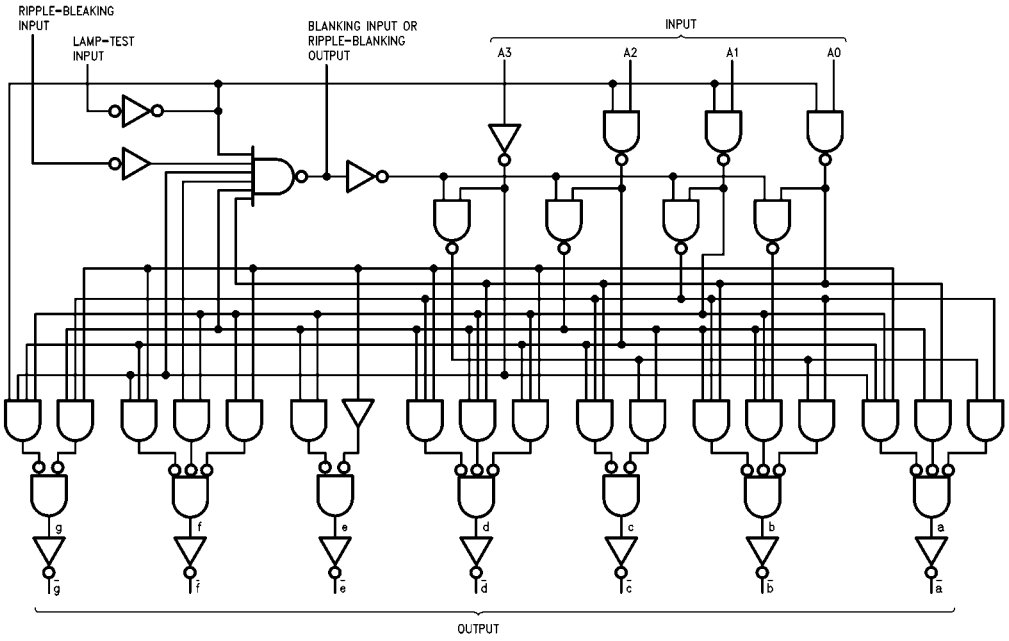
Note 4: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 5: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

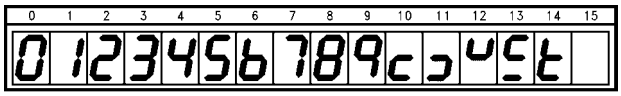
Functional Description

The DM74LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multi-digit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{RBI}$ of a intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $\overline{BI/RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

Logic Diagram



Numerical Designations—Resultant Displays



FAIRCHILD SEMICONDUCTOR TM

March 1998

DM7476
Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

General Description

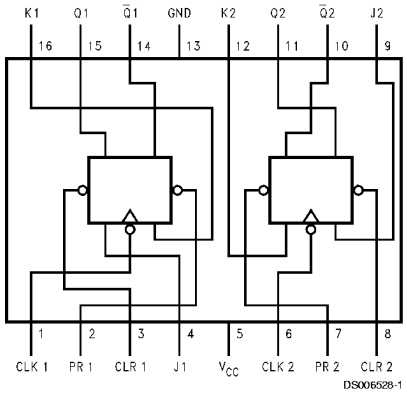
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5476) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5476DMQB, 5476FMQB, DM5476J, DM5476W or DM7476N
See Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

DATA SHEET

74F85
4-bit magnitude comparator

Product specification

1994 Sep 27

IC15 Data Handbook

Philips Semiconductors

PHILIPS

4-bit magnitude comparator 74F85

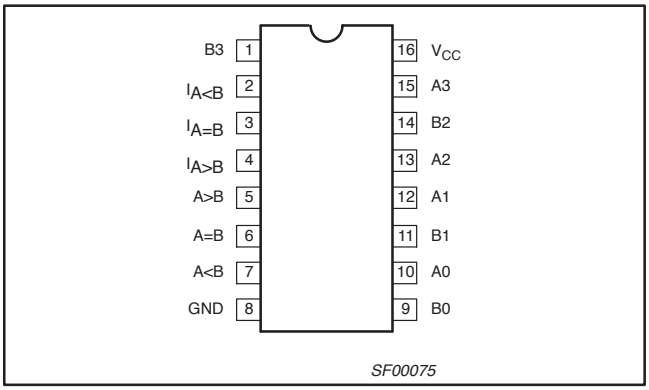
FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating

DESCRIPTION

The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs $I_{A>B}$, and $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the lease significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING INFORMATION

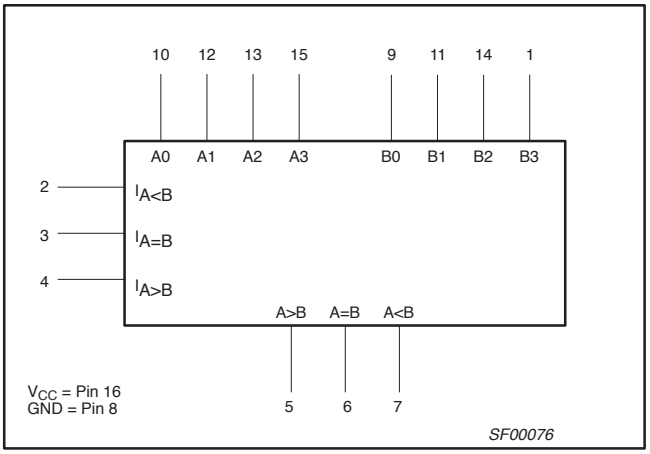
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F85N	SOT38-4
16-pin plastic SO	N74F85D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

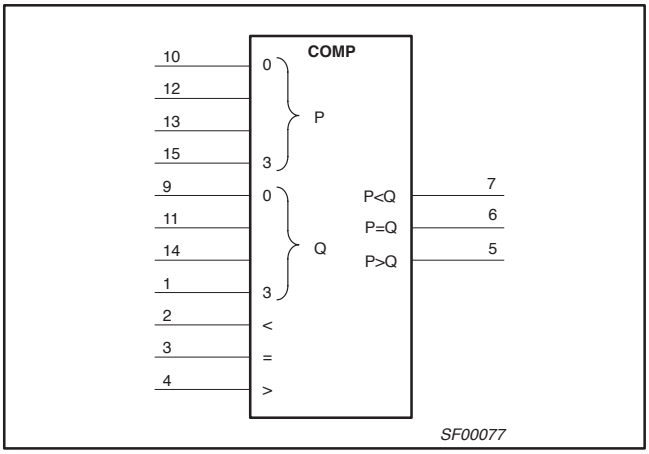
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A3	Comparing inputs	1.0/0.033	20μA/20μA
B0–B3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active High)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active High)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

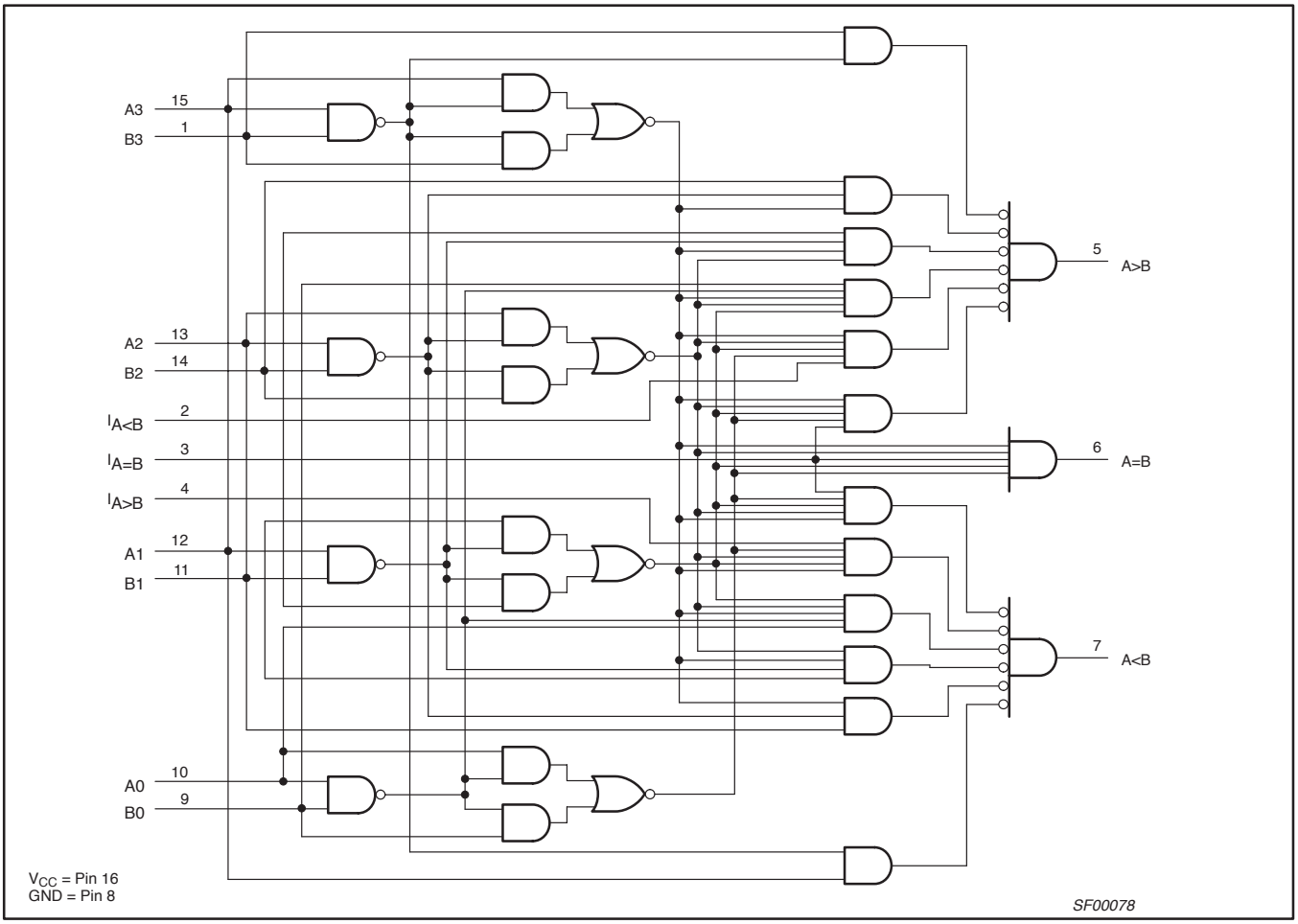
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

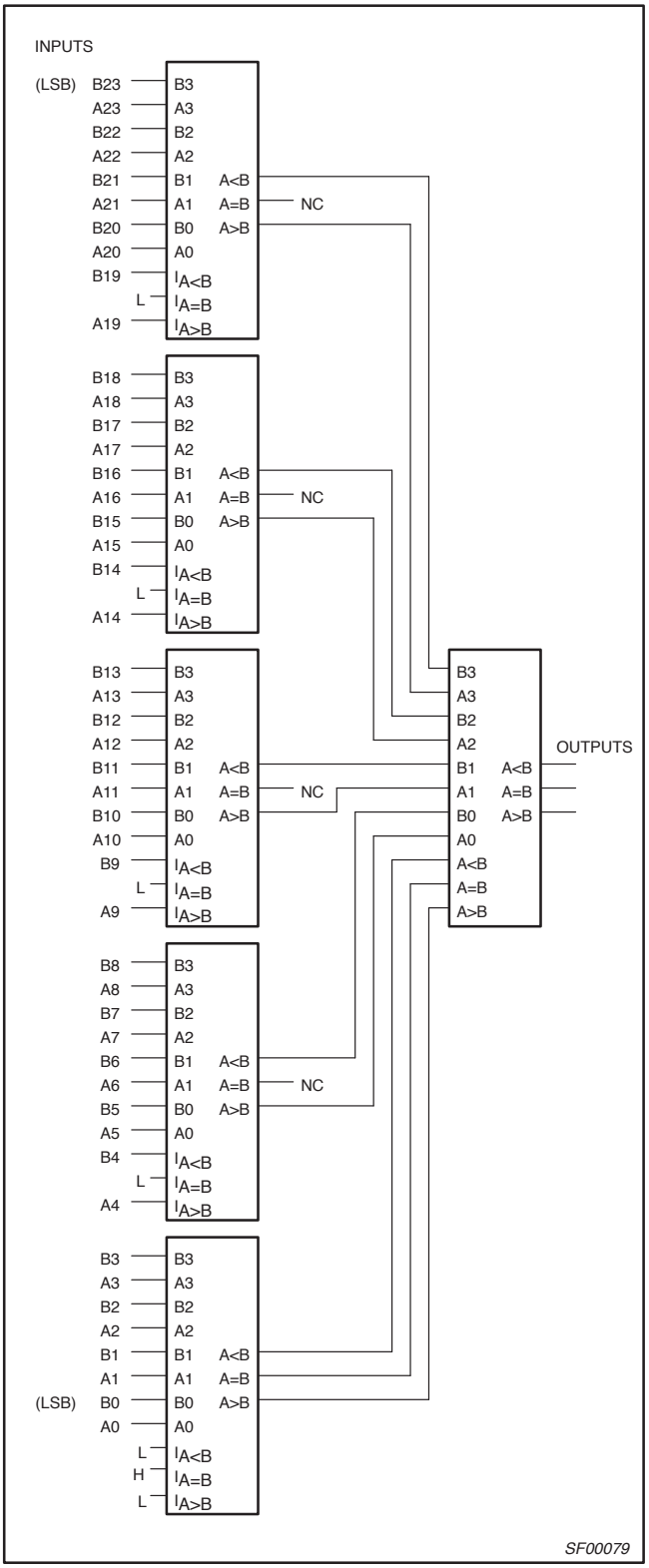


Figure 1. Comparison of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device, which must be connected as in the serial scheme. The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ = Low. The 74F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A0–A3) and (B0–B3) inputs of another 74F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1–4 bits	1	12ns
5–24 bits	2–6	22ns
25–120 bits	8–31	34ns

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		36	50	mA
	Supply current (total) I_{CCL}	V_{CC} = MAX	An = Bn = $I_{A=B}$ = GND, $I_{A>B}$= $I_{A<B}$ = 4.5V		40	54	mA

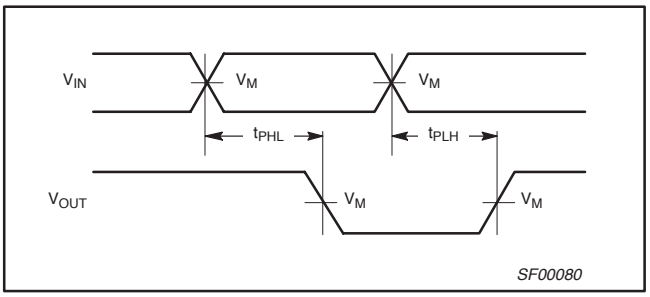
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A or B to A<B, A>B	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to A=B	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ to A=B	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

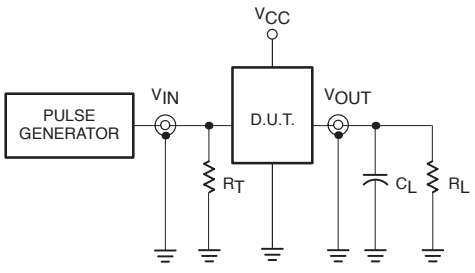
AC WAVEFORMS



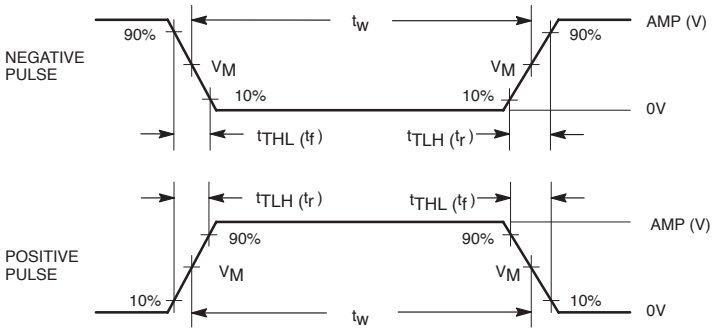
Waveform 1. Propagation Delay Input to Output

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

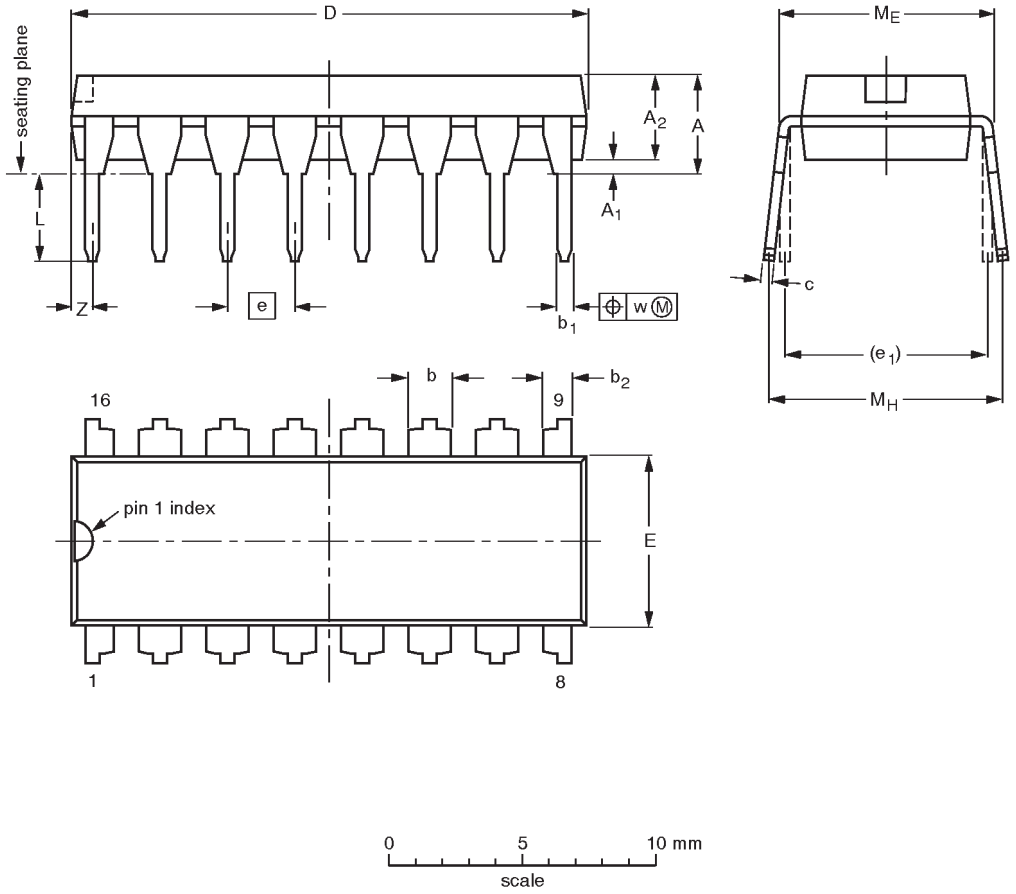
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

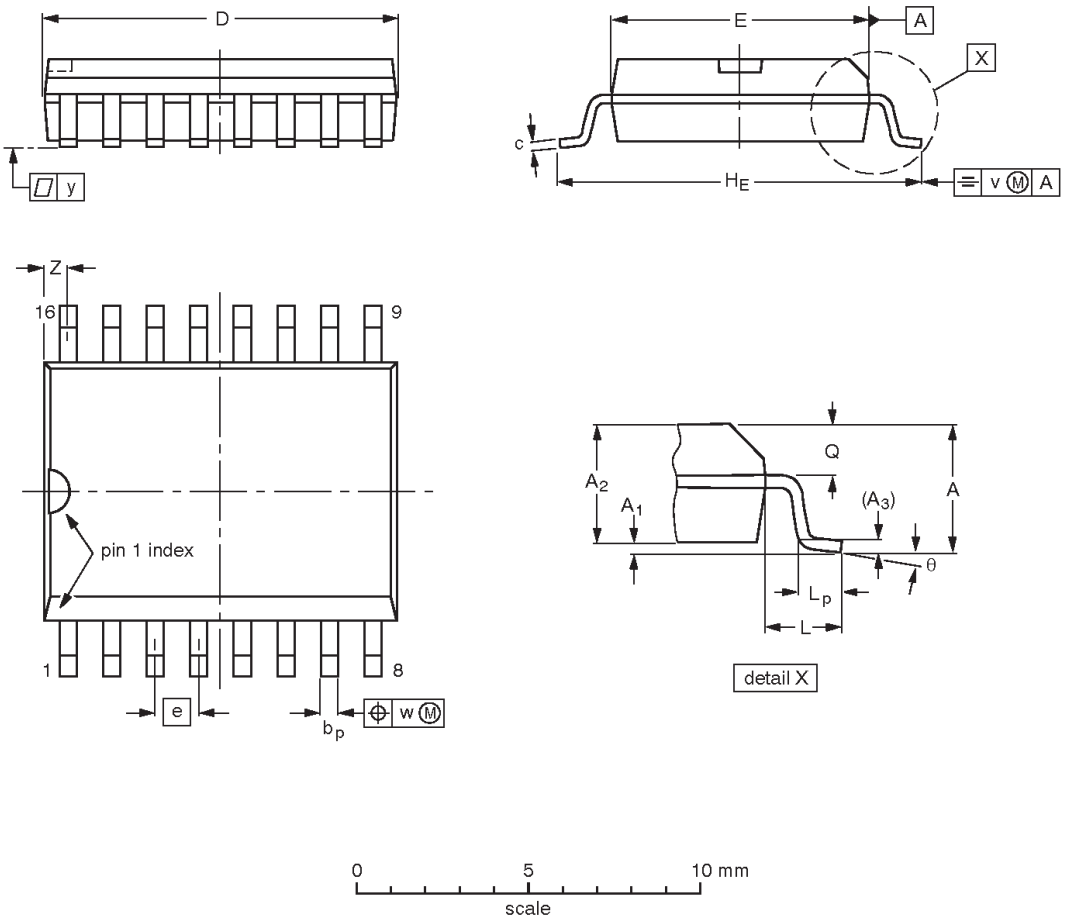
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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print code Date of release: 10-98

Document order number: 9397-750-05067

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September 1986
Revised February 2000

DM7486
Quad 2-Input Exclusive-OR Gate

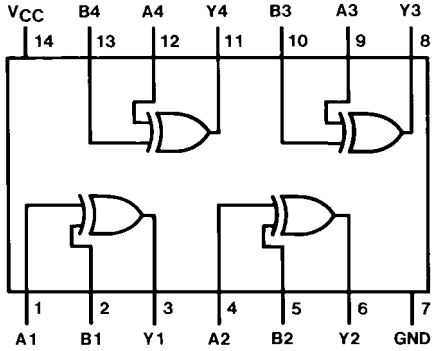
General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM7486N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

8-input multiplexer 74HC/HCT151

FEATURES

- True and complement outputs
- Multifunction capability
- Permits multiplexing from n lines to 1 line
- Non-inverting data path
- See the “251” for the 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	I_n to Y, $\overline{Y}$		17	19	ns
	S_n to Y, $\overline{Y}$		19	20	ns
	$\overline{E}$ to Y		12	13	ns
	$\overline{E}$ to $\overline{Y}$		14	18	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

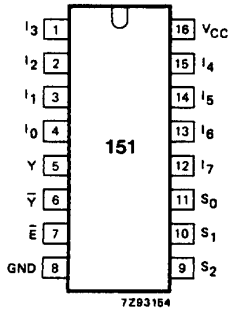


Fig.1 Pin configuration.

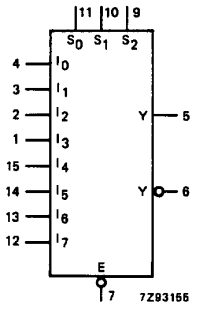


Fig.2 Logic symbol.

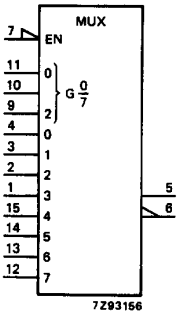


Fig.3 IEC logic symbol.

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care.

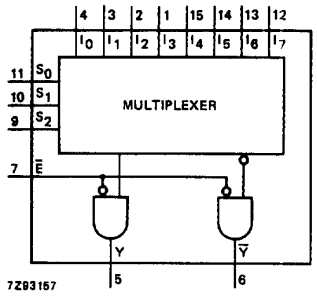


Fig.4 Functional diagram.

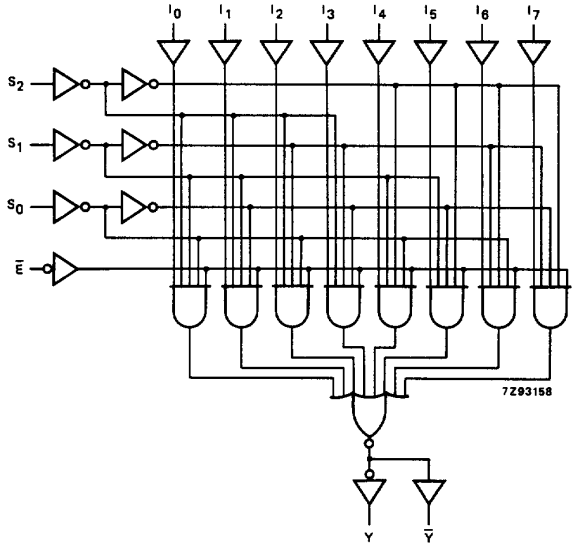


Fig.5 Logic diagram.

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised July 2001

DM74164
8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A LOW logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the LOW level at the next clock pulse, thus providing complete control over incoming data. A HIGH logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the LOW-to-HIGH level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

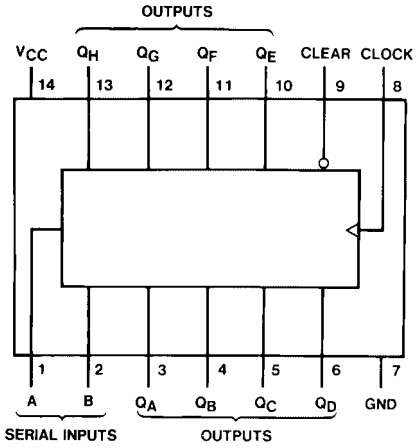
Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74164	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

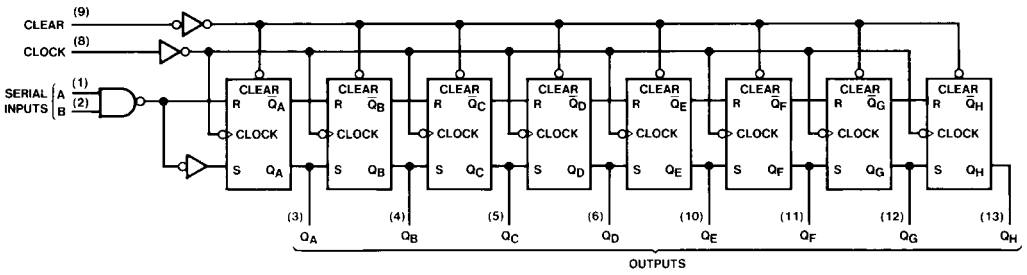


Function Table

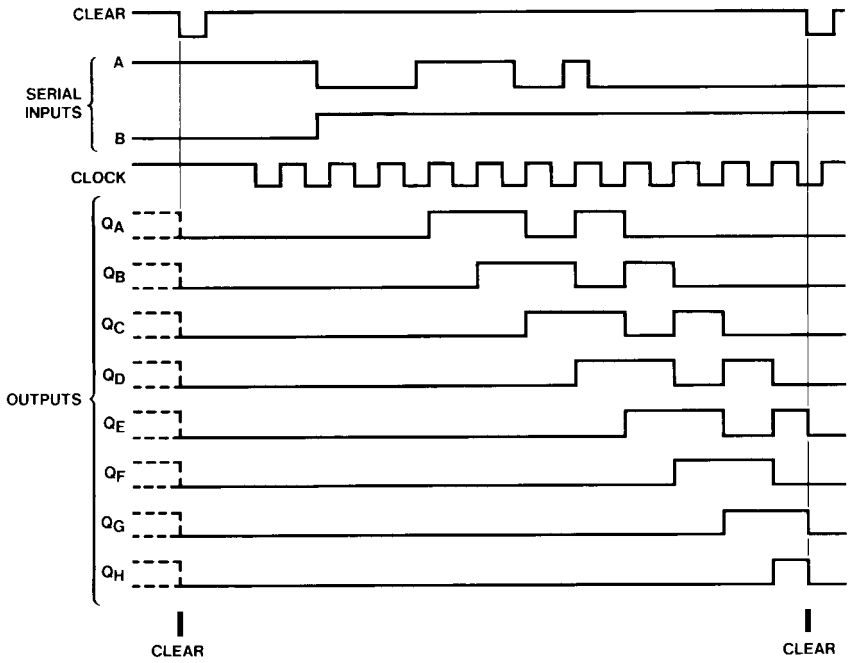
Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	…	Q_H
L	X	X	X	L	L	…	L
H	L	X	X	Q_{A0}	Q_{B0}	…	Q_{H0}
H	↑	H	H	H	Q_{An}	…	Q_{Gn}
H	↑	L	X	L	Q_{An}	…	Q_{Gn}
H	↑	X	L	L	Q_{An}	…	Q_{Gn}

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



Timing Diagram



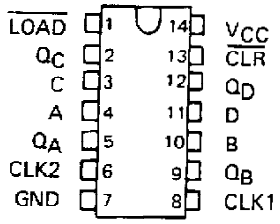
SDLS069

SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

MAY 1971—REVISED MARCH 1988

- Reduced-Power Versions of SN54196, SN54197, SN74196, and SN74197 50-MHz Counters
- D-C Coupled Counters Designed to Replace Signetics 8280, 8281, 8290, and 8291 Counters In Most Applications
- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Counts at Input Frequencies from 0 to 35 MHz
- Input Clamping Diodes Simplify System Design

SN54176, SN54177 . . . J PACKAGE
SN74176, SN74177 . . . N PACKAGE
(TOP VIEW)



description

These high-speed monolithic counters consist of four d-c coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54176, SN74176) or a divide-by-two and a divide-by-eight counter (SN54177, SN74177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

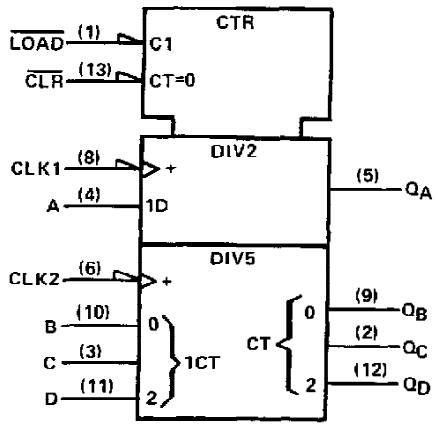
These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

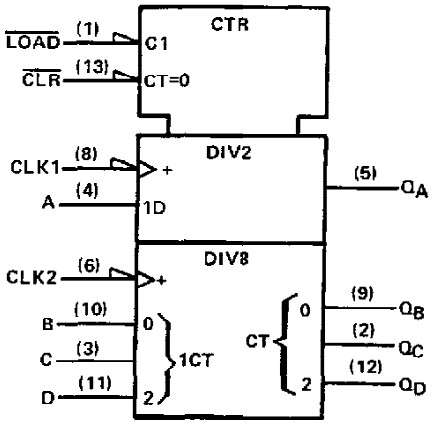
All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The circuits are compatible with most TTL logic families. Typical power dissipation is 150 milliwatts. The SN54176 and SN54177 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74176 and SN74177 circuits are characterized for operation from 0°C to 70°C.

logic symbols†

'176



'177



† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

typical count configurations

SN54176 and SN74176

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.

FUNCTION TABLES
SN54176, SN74176

DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54177 and SN74177

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the function table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

FUNCTION TABLE
SN54177, SN74177
(See Note A)

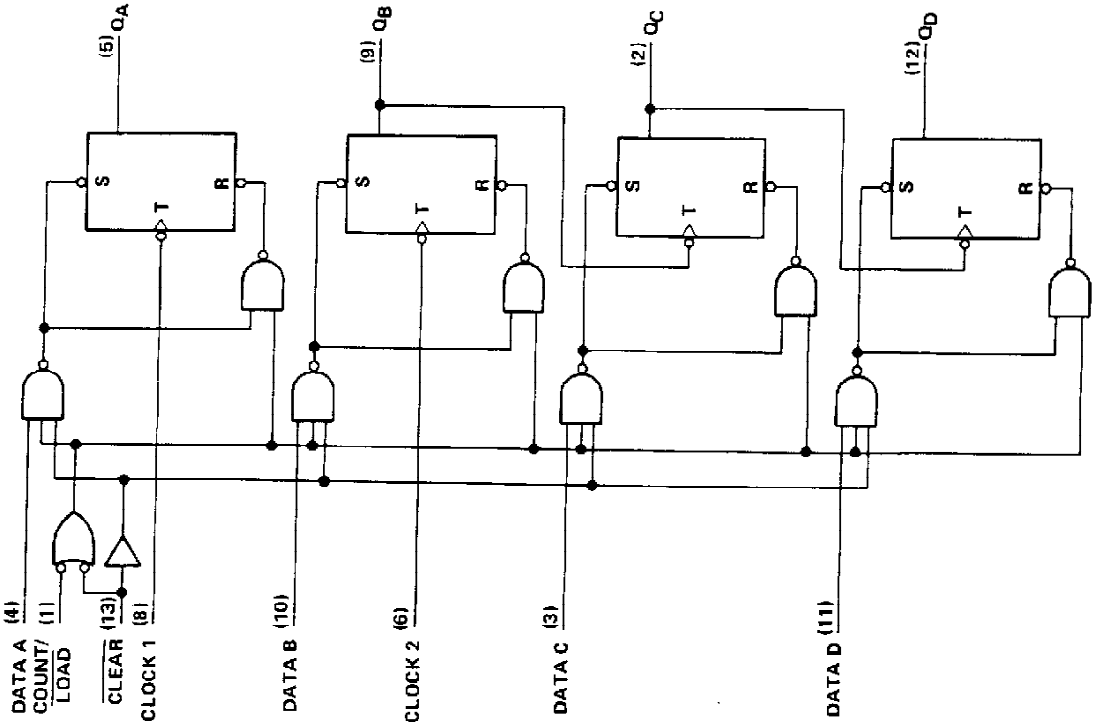
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level

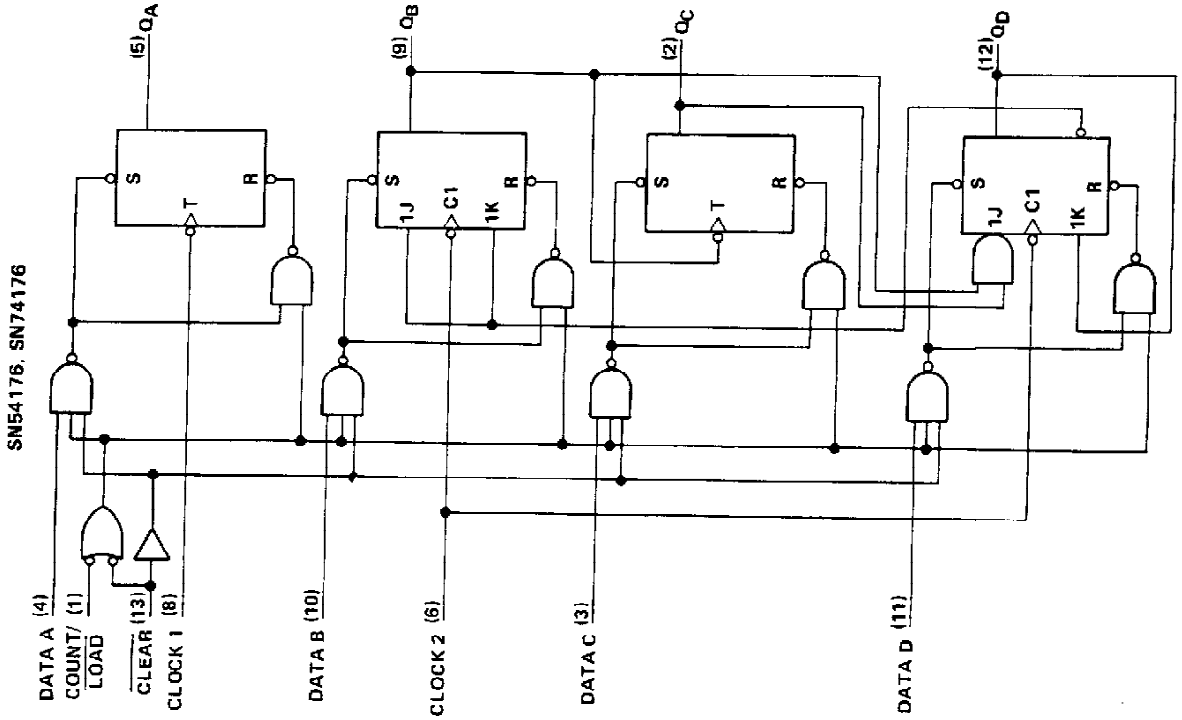
NOTE A: Output Q_A connected to clock-2 input.

logic diagrams (positive logic)

SN54177, SN74177



SN54176, SN74176



DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT181
4-bit arithmetic logic unit

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

1998 Jun 10

Philips
Semiconductors

PHILIPS

4-bit arithmetic logic unit 74HC/HCT181

FEATURES

- Full carry look-ahead for high-speed arithmetic operation on long words
- Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others
- Provides all 16 logic operations of two variables: EXCLUSIVE-OR, compare, AND, NAND, NOR, OR plus 10 other logic operations
- Output capability: standard, A=B open drain
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT181 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT181 are 4-bit high-speed parallel Arithmetic Logic Units (ALU). Controlled by the four function select inputs (S_0 to S_3) and the mode control input (M), they can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands (see function table).

When the mode control input (M) is HIGH, all internal carries are inhibited and the device3 performs logic operations on the individual bits as listed. When M is LOW, the carries are enabled and the "181" performs arithmetic operations on the two 4-bit words. The "181" incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the carry propagation ($\overline{P}$) and carry generate ($\overline{G}$) signals. $\overline{P}$ and $\overline{G}$ are not affected by carry in.

When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output (C_{n+4}) signal to the carry input (C_n) of the next unit.

For high-speed operation the device is used in conjunction with the "182" carry look-ahead circuit. One carry look-ahead package is required for each group of four "181" devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The comparator output (A=B) of the device goes HIGH when all four function outputs ($\overline{F}_0$ to $\overline{F}_3$) are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. A=B is an open collector output and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The open drain output A=B should be used with an external pull-up resistor in order to establish a logic HIGH level. The A=B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no under-flow and no carry is generated when there is underflow.

As indicated, the "181" can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs.
For either case the table lists the operations that are performed to the operands.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC181N3; 74HCT181N3	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
74HC181N; 74HCT181N	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
74HC181D; 74HCT181D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	$\overline{A}_n$ or $\overline{B}_n$ to A=B		28	30	ns
	C_n to $C_{n+}4$		17	21	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per L package	notes 1 and 2	90	92	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

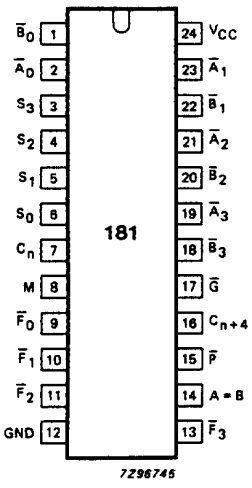


Fig.1 Pin configuration.

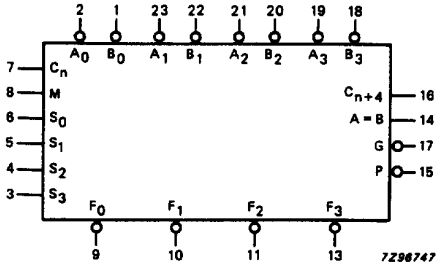


Fig.2 Logic symbol.

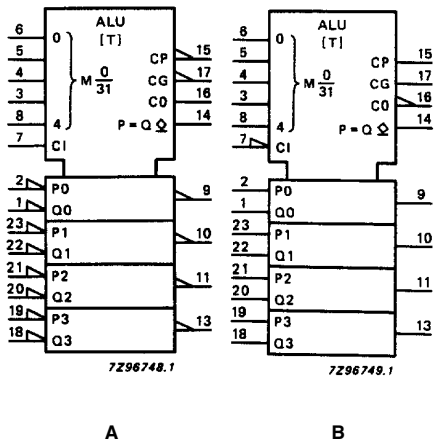


Fig.3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\overline{B}_0$ to $\overline{B}_3$	operand inputs (active LOW)
2, 23, 21, 19	$\overline{A}_0$ to $\overline{A}_3$	operand inputs (active LOW)
6, 5, 4, 3	S_0 to S_3	select inputs
7	C_n	carry input
8	M	mode control input
9, 10, 11, 13	$\overline{F}_0$ to $\overline{F}_3$	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	$\overline{P}$	carry propagate output (active LOW)
16	C_{n+4}	carry output
17	$\overline{G}$	carry generate output (active LOW)
24	V_{CC}	positive supply voltage

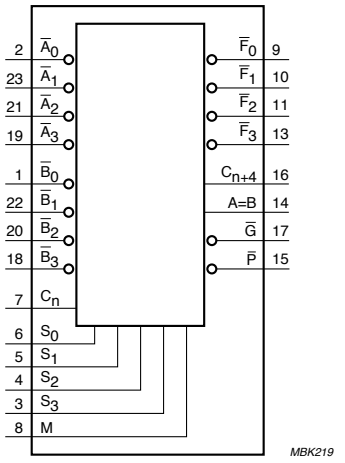


Fig.4 Functional diagram.

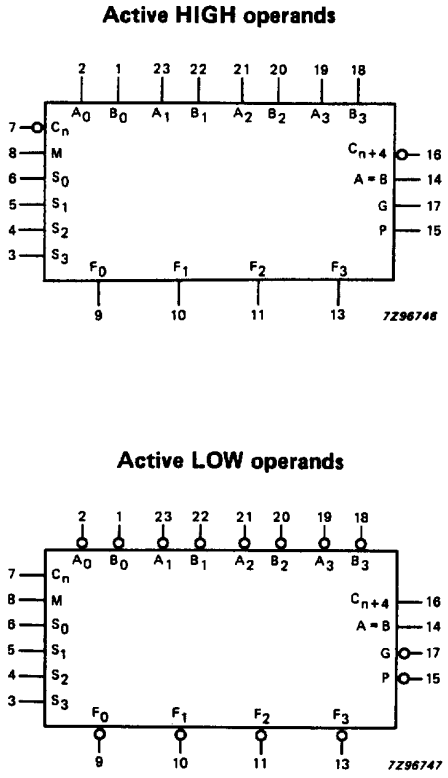


Fig.5 Active HIGH operands - active LOW operands.

FUNCTION TABLES

MODE SELECT INPUTS				ACTIVE HIGH INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC[2] (M=L; C_n=H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	A $\oplus$ B	A minus B minus 1
L	H	H	H	A$\overline{B}$	A$\overline{B}$ minus 1
H	L	L	L	$\overline{A}$ + B	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	logical 1	A plus A[1]
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC[2] (M=L; C_n=L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	logical 1	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}$B	A plus (A + B)
H	L	L	H	A $\oplus$ B	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	logical 0	A plus A[1]
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

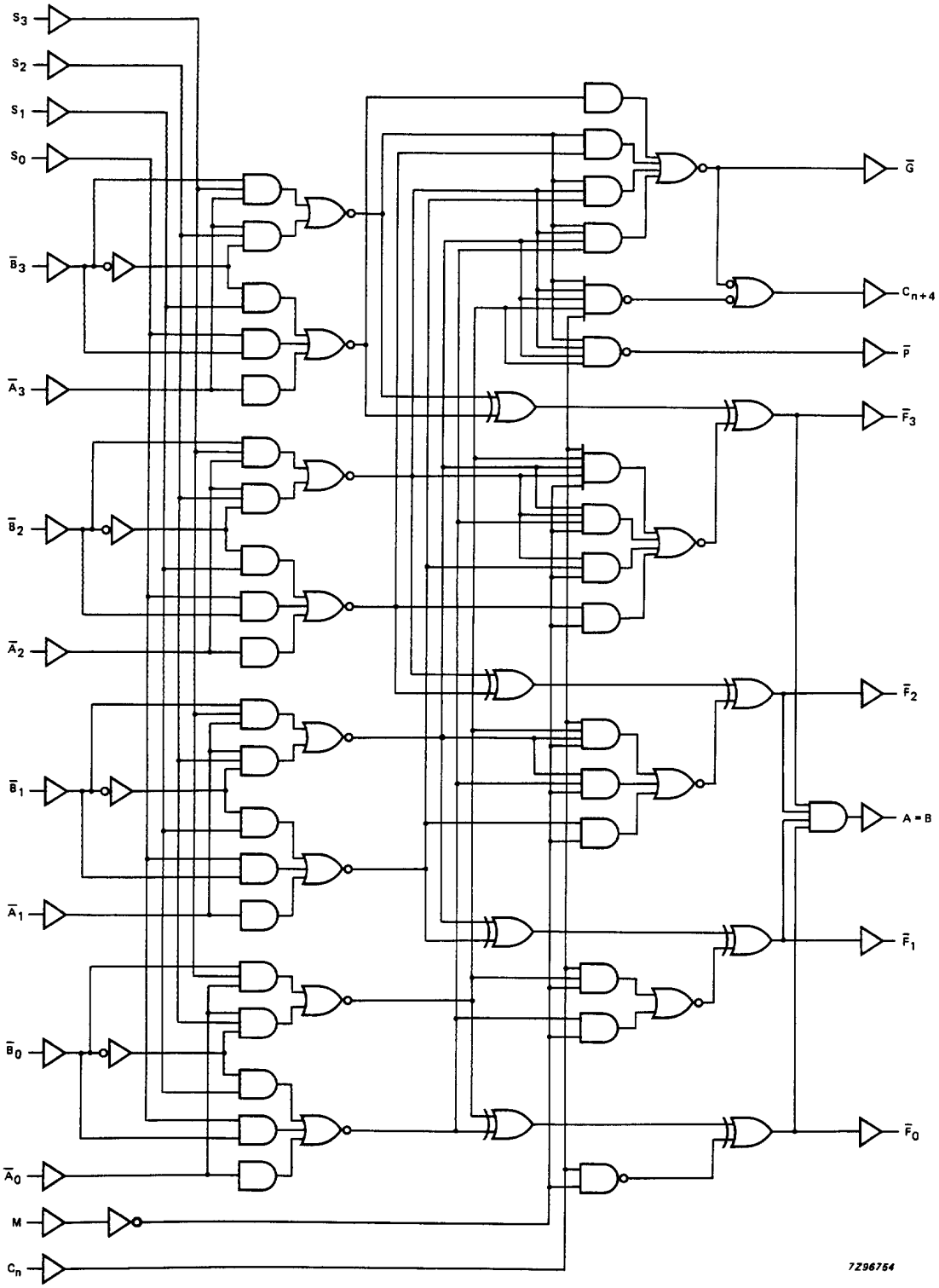


Fig.6 Logic diagram.

Table 1 SUM MODE TEST

Function inputs $S_0 = S_3 = 4.5$ V, $M = S_1 = S_2 = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH}/ t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}/ t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/ t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}/ t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}/ t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}/ t_{PHL}	C_n	none	none	all $\overline{A}$	all $\overline{B}$	any $\overline{F}$ or C_{n+4}

Table 2 DIFFERENTIAL MODE TEST

Function inputs $S_1 = S_2 = 4.5$ V, $M = S_0 = S_3 = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH}/ t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{A}$	remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	remaining $\overline{A}$	remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}/ t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/ t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLZ}/ t_{PZL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{A}$	remaining $\overline{B}$, C_n	A=B
t_{PLZ}/ t_{PZL}	$\overline{B}_i$	$\overline{A}_i$	none	remaining $\overline{A}$	remaining $\overline{B}$, C_n	A=B
t_{PLH}/ t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH}/ t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	none	remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH}/ t_{PHL}	C_n	none	none	all $\overline{A}$ and $\overline{B}$	none	any $\overline{F}$ or C_{n+4}

Table 3 LOGIC MODE TEST

Function inputs $M = S_1 = S_2 = 4.5$ V, $S_0 = S_3 = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH}/ t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}/ t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$

RATINGS (for A=B output only)
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_O	DC output voltage	−0.5	+7.0	V	
$-I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V
$-I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O$

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_{IL}	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	μA	2.0 to 6.0	V_{IL}	note 1 V_O = 0 or 6 V

Note to the DC characteristics

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay C_n to C_{n+4}		55 20 16	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	sum diff	M = 0 V; Fig.9; Tables 1 and 2
t_{PHL}/ t_{PLH}	propagation delay C_n to $\overline{F}_n$		69 25 20	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	sum diff	M = 0 V; Fig.9; Tables 1 and 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		72 26 21	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		77 28 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		76 26 21	215 43 37		270 54 46		320 65 55	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		77 28 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		85 31 25	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		83 31 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	logic	M = 4.5 V; Fig.8; Table 3
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	logic	M = 4.5 V; Fig.8; Table 3
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		80 29 23	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.8; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		80 29 23	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.8; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.10; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		85 31 25	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.10; Table 2
t_{PZL}/ t_{PLZ}	propagation delay $\overline{A}_n$ to A=B		80 29 23	245 49 42		305 61 52		370 74 63	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.11; Table 2
t_{PZL}/ t_{PLZ}	propagation delay $\overline{B}_n$ to A=B		88 32 26	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.11; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{F}_n$		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{F}_n$		88 32 26	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0		note ; Figs 7 and 11

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_{IL}	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	μA	2.0 to 6.0	V_{IL}	note 1 V_O = 0 or 6 V

Note to the DC characteristics

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
C_n, M	0.50
$\overline{A}_n$, $\overline{B}_n$	0.75
S_n	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay C_n to C_{n+4}		25	42		53		63	ns	4.5	sum diff	M = 0 V; Fig.9; Tables 1 and 2
t_{PHL}/ t_{PLH}	propagation delay C_n to $\overline{F}_n$		28	48		60		72	ns	4.5	sum diff	M = 0 V; Fig.9; Tables 1 and 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		31	54		68		81	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		32	54		68		81	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		31	54		68		81	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		31	54		68		81	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		23	41		51		62	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		24	41		51		62	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		23	40		50		60	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		23	40		50		60	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		33	58		73		87	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		34	58		73		87	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		33	57		71		86	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		33	57		71		86	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		29	54		68		81	ns	4.5	logic	M = 4.5 V; Fig.8; Table 3
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		33	54		68		81	ns	4.5	logic	M = 4.5 V; Fig.8; Table 3
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		30	53		66		80	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.8; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		31	53		66		80	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.8; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		30	55		69		83	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.10; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		34	55		69		83	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.10; Table 2
t_{PZL}/ t_{PLZ}	propagation delay $\overline{A}_n$ to A=B		34	60		75		90	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.11; Table 2
t_{PZL}/ t_{PLZ}	propagation delay $\overline{B}_n$ to A=B		35	60		75		90	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.11; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		33	56		70		84	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{F}_n$		33	56		70		84	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig.7; Table 1

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		32	56		70		84	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		33	56		70		84	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig.8; Table 2
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5		Figs 7 and 11; note 1

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

AC WAVEFORMS

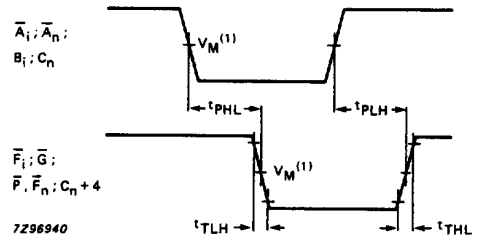


Fig.7 Propagation delays for carry input to carry output, carry input to function outputs, operands to carry generate operands, propagation outputs and output transition lines.

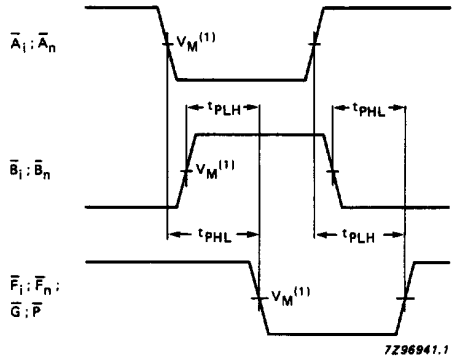


Fig.8 Propagation delays for operands to carry generate, propagate outputs and function outputs.

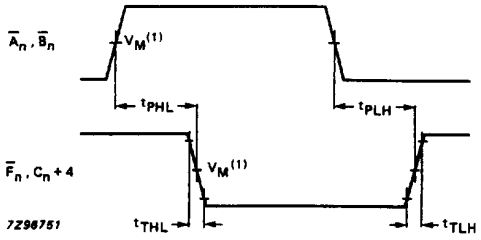


Fig.9 Propagation delays for operands to carry output and function outputs.

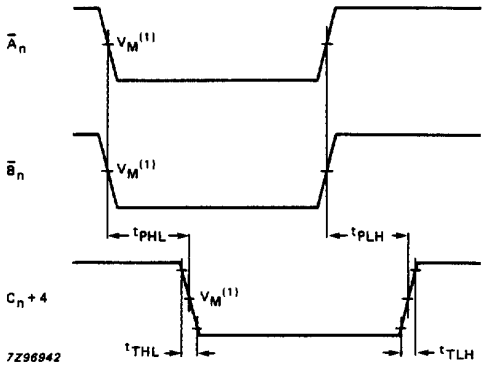


Fig.10 Propagation delays for operands to carry output.

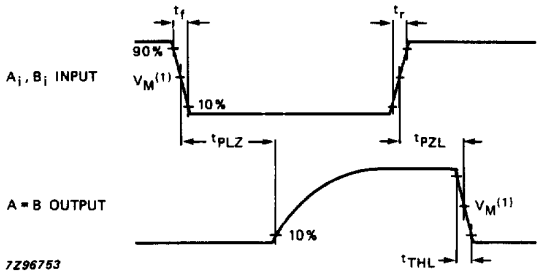
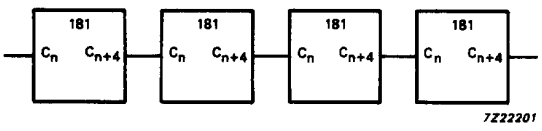


Fig.11 Waveforms showing the input (A_i, B_j) to output (A=B) propagation delays and output transition time of the open drain output (A=B).

Note to AC waveforms

(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

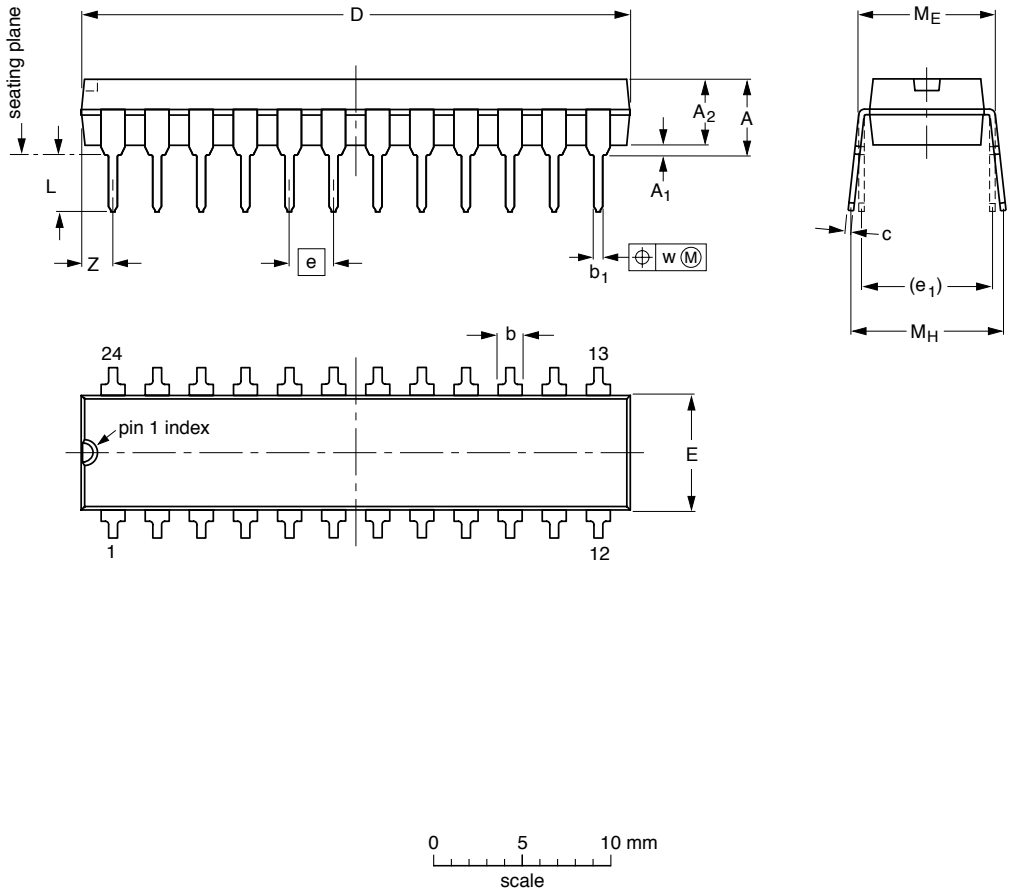


A and B inputs and F outputs of "181" are not shown

Fig.12 Application example showing 16-bit ALU ripple-carry configuration.

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

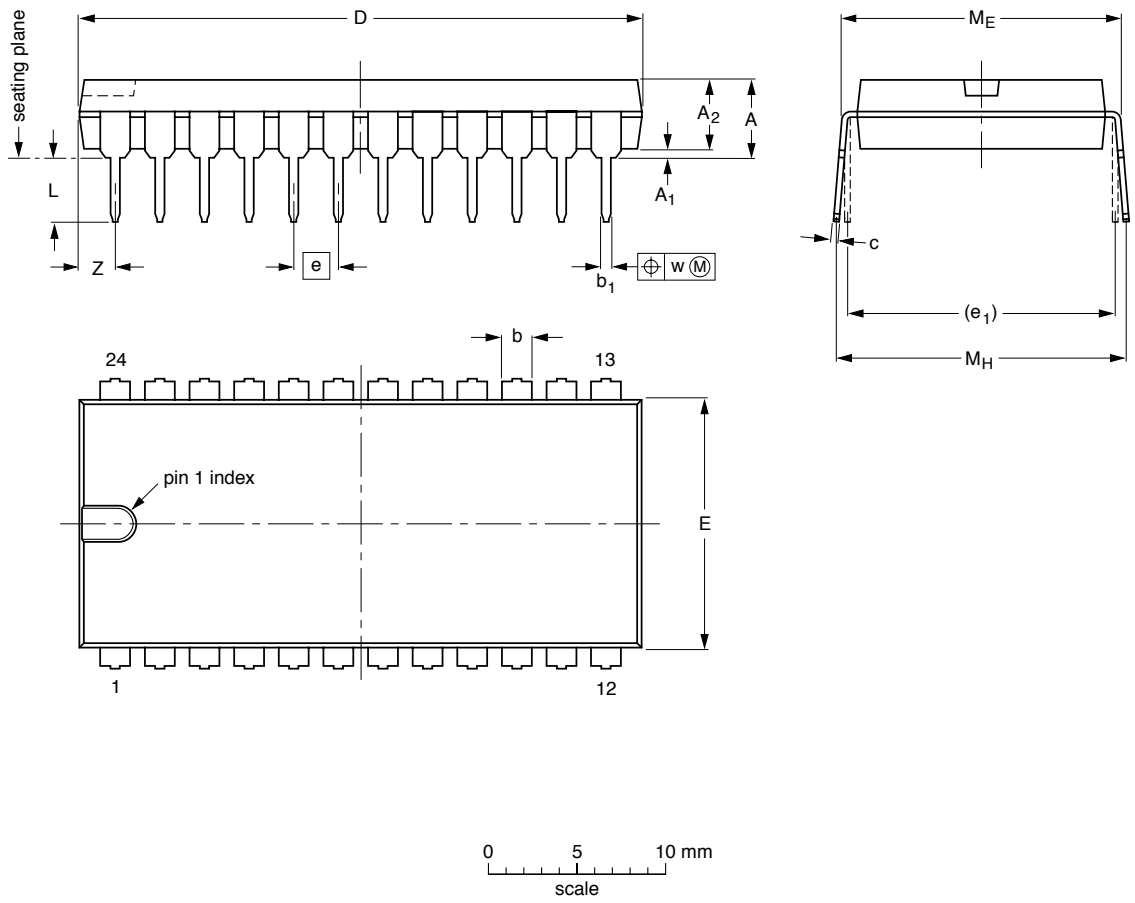
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

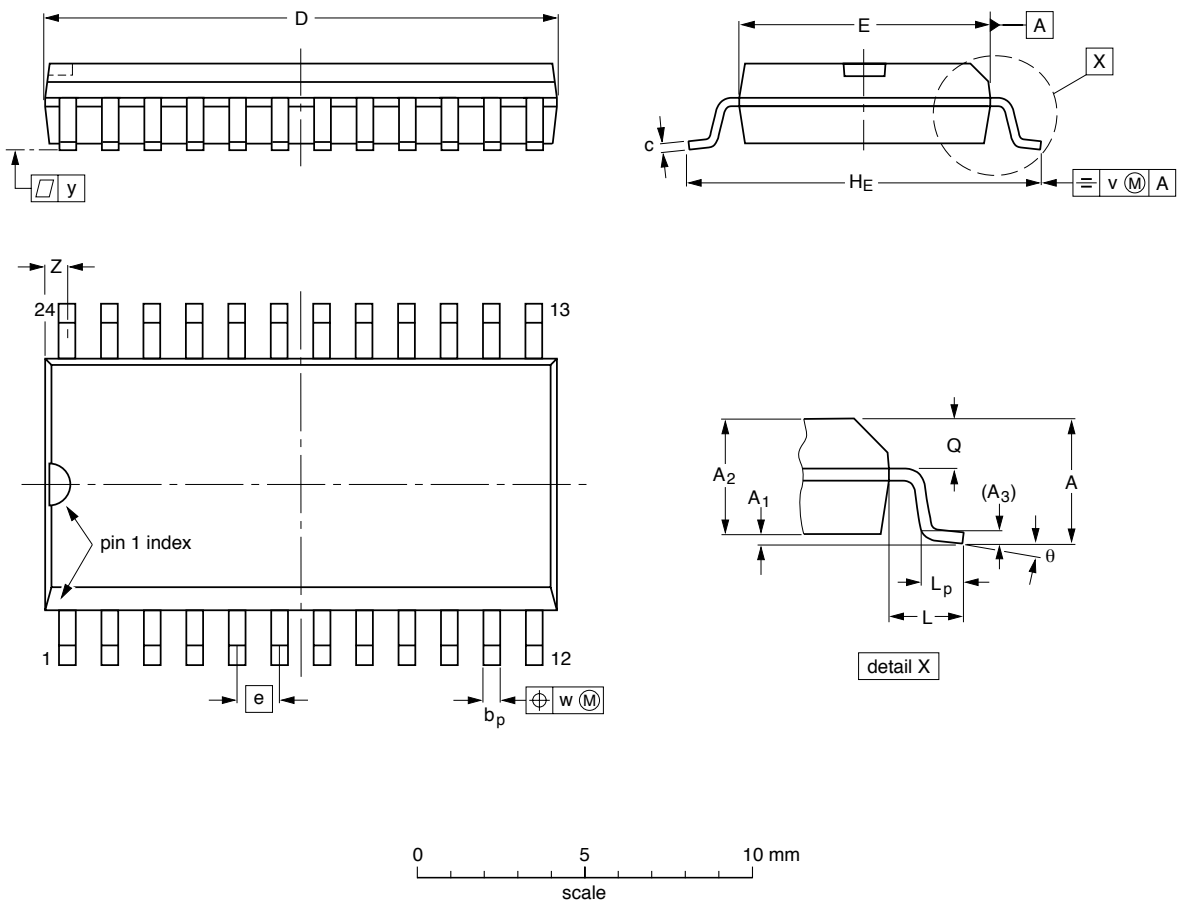
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

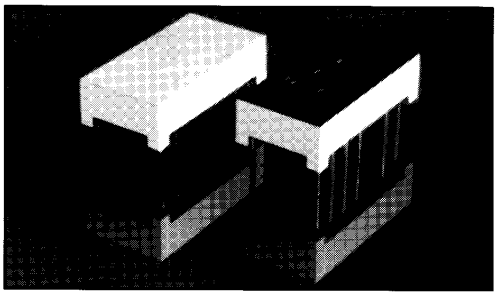
LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

FAIRCHILD
SEMICONDUCTOR™

0.300-INCH SEVEN SEGMENT DISPLAYS

HIGH EFFICIENCY GREEN MAN3400A
ORANGE MAN3600A
RED MAN70A
YELLOW MAN3800A



DESCRIPTION

The MAN3400A, MAN3600A, MAN70A and MAN3800A Series provides a choice of color of LED displays. Standard units are available in Red, Green, Orange and Yellow. They can be mounted in arrays with 0.400-inch (10.16 mm) center-to-center spacing. Yellow and High Efficiency Green displays are constructed with Grey face and neutral segment color. Red displays have Black faces and Red segment color. Others have face and segment color corresponding to the emitted light.

FEATURES

- Common anode or common cathode models
- Red, Yellow, Green and Orange
- Fast switching — excellent for multiplexing
- Low power consumption
- Bold solid segments that are highly legible
- Solid state reliability — long operation life
- Impact resistant plastic construction
- Directly compatible with integrated circuits
- High brightness with high contrast
- Categorized for Luminous Intensity (See Note 6)
- Standard 14 pin dual-in-line package configuration
- Wide angle viewing...150°

APPLICATIONS

- Digital readout displays
- Instrument panels
- Point of sale equipment
- Calculators
- Digital clocks

MODEL NUMBERS

PART NUMBER	COLOR	DESCRIPTION
MAN3410A	High Efficiency Green	Common Anode; Right Hand Decimal
MAN3420A	High Efficiency Green	Common Anode; Left Hand Decimal
MAN3440A	High Efficiency Green	Common Cathode; Right Hand Decimal
MAN3610A	Orange	Common Anode; Right Hand Decimal
MAN3620A	Orange	Common Anode; Left Hand Decimal
MAN3630A	Orange	Common Anode; Overflow ±1
MAN3640A	Orange	Common Cathode; Right Hand Decimal
MAN71A	Red	Common Anode; Right Hand Decimal
MAN72A	Red	Common Anode; Left Hand Decimal
MAN73A	Red	Common Anode; Overflow ±1
MAN74A	Red	Common Cathode; Right Hand Decimal
MAN3810A	Yellow	Common Anode; Right Hand Decimal
MAN3820A	Yellow	Common Anode; Left Hand Decimal
MAN3840A	Yellow	Common Cathode; Right Hand Decimal

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ELECTRO-OPTICAL CHARACTERISTICS

(25°C Free Air Temperature Unless Otherwise Specified)

	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
MAN3410A, 3420A, 3440A					
Luminous Intensity, digit average	750	3200		μcd	I_F=10 mA
(See Notes 1 and 3)	900	4000		μcd	I_F=60 mA peak, 1:6 DF
Peak emission wavelength		562		nm	
Spectral line half width		30		nm	
Forward voltage					
Segment		2.2	3.0	V	I_F=20 mA
Decimal point		2.2	3.0	V	I_F=20 mA
Dynamic resistance					
Segment		12		Ω	I_F=20 mA
Decimal point		12		Ω	I_F=20 mA
Capacitance					
Segment		40		pF	V=0
Decimal point		40		pF	V=0
Reverse current					
Segment			100	μA	V_R=5.0 V
Decimal point			100	μA	V_R=5.0 V
MAN3610A, 3620A, 3630A, 3640A					
Luminous Intensity, digit average	510	1800		μcd	I_F=10 mA
(See Note 1 and 3)					
Peak emission wavelength		630		nm	
Spectral line half width		40		nm	
Forward voltage					
Segment			2.5	V	I_F=20 mA
Decimal point			2.5	V	I_F=20 mA
Dynamic resistance					
Segment		26		Ω	I_F=20 mA
Decimal point		26		Ω	I_F=20 mA
Capacitance					
Segment		35		pF	V=0
Decimal point		35		pF	V=0
Reverse current					
Segment			100	μA	V_R=5.0 V
Decimal point			100	μA	V_R=5.0 V

ELECTRO-OPTICAL CHARACTERISTICS
(25°C Free Air Temperature Unless Otherwise Specified) (Cont'd)

	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
MAN71A, 72A, 73A, 74A					
Luminous Intensity, digit average (See Note 1 and 3)	125	350		μcd	I_F=10 mA
Peak emission wavelength		660		nm	
Spectral line half width		20		nm	
Forward voltage					
Segment			2.0	V	I_F=20 mA
Decimal point			2.0	V	I_F=20 mA
Dynamic resistance					
Segment		2		Ω	I_{pk}=100 mA
Decimal point		2		Ω	I_{pk}=100 mA
Capacitance					
Segment		35	80	pF	V=0
Decimal point		35	80	pF	V=0
Reverse current					
Segment			100	μA	V_R=5.0 V
Decimal point			100	μA	V_R=5.0 V
MAN3810A, 3820A, 3840A					
Luminous Intensity, digit average (See Note 1 and 3)	450	1700		μcd	I_F=10 mA
Peak emission wavelength		585		nm	
Spectral line half width		40		nm	
Forward voltage					
Segment			3.0	V	I_F=20 mA
Decimal point			3.0	V	I_F=20 mA
Dynamic resistance					
Segment		26		Ω	I_F=20 mA
Decimal point		26		Ω	I_F=20 mA
Capacitance					
Segment		35		pF	V=0
Decimal point		35		pF	V=0
Reverse current					
Segment			100	μA	V_R=5.0 V
Decimal point			100	μA	V_R=5.0 V

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RECOMMENDED OPTICAL FILTERS

For optimum ON and OFF contrast, one of the following filters or equivalents should be used over the display:

DEVICE TYPE	FILTER	DEVICE TYPE	FILTER
MAN3610A MAN3620A MAN3630A MAN3640A	Panelgraphic Scarlet 65 Homalite 100-1670	MAN71A MAN72A MAN73A MAN74A	Panelgraphic Red 60 Homalite 100-1605
MAN3410A MAN3420A MAN3440A	Panelgraphic Green 48 Homalite 100-1440 Green	MAN3810A MAN3820A MAN3840A	Panelgraphic Yellow 25 or Amber 23 Homalite 100-1720 or 100-1726 Panelgraphic Grey 10 Homalite 100-1266 Grey

ABSOLUTE MAXIMUM RATINGS

	HIGH EFF. GREEN MAN3410A MAN3420A MAN3440A	RED MAN71A MAN72A MAN74A	 MAN73A
Power dissipation at 25°C ambient	600 mW	480 mW	300 mW
Derate linearly from 50°C	−12 mW/°C	−6.9 mW/°C	−4.29 mW/°C
Storage and operating temperature	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C
Continuous forward current			
Total	240 mA	240 mA	150 mA
Per segment	30 mA	30 mA	30 mA
Decimal point	30 mA	30 mA	30 mA
Reverse voltage			
Per segment	6.0 V	6.0 V	6.0 V
Decimal point	6.0 V	6.0 V	6.0 V
Soldering time at 260°C (See Notes 4 and 5)	5 sec.	5 sec.	5 sec.

	YELLOW MAN3810A MAN3820A MAN3840A	ORANGE MAN3610A MAN3620A MAN3640A	 MAN3630A
Power dissipation at 25°C ambient	600 mW	600 mW	375 mW
Derate linearly from 50°C	−10.3 mW/°C	−8.6 mW/°C	−5.36 mW/°C
Storage and operating temperature	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C
Continuous forward current			
Total	200 mA	240 mA	150 mA
Per segment	25 mA	30 mA	30 mA
Decimal point	25 mA	30 mA	30 mA
Reverse voltage			
Per segment	6.0 V	6.0 V	6.0 V
Decimal point	6.0 V	6.0 V	6.0 V
Soldering time at 260°C (See Notes 4 and 5)	5 sec.	5 sec.	5 sec.

TYPICAL THERMAL CHARACTERISTICS

GREEN/YELLOW

Thermal resistance junction to free air Φ_{JA} . . . . . 160°C/W
Wavelength temperature coefficient (case temperature) . . . . . 1.0Å/°C
Forward voltage temperature coefficient . . . . . −1.5 mV/°C

RED/ORANGE

Thermal resistance junction to free air Φ_{JA} . . . . . 160°C/W
Wavelength temperature coefficient (case temperature) . . . . . 1.0Å/°C
Forward voltage temperature coefficient . . . . . −2.0 mV/°C

NOTES

1. *The digit average Luminous Intensity is obtained by summing the Luminous Intensity of each segment and dividing by the total number of segments. Intensity will not vary more than ±33.3% between all segments within a digit.*
2. *The curve in Figures 3, 6, 9, and 12 is normalized to the brightness at 25°C to indicate the relative Luminous Intensity over the operating temperature range.*
3. *The decimal point is designed to have the same surface brightness as the segments, therefore, the Luminous Intensity of the decimal point is .3 times the Luminous Intensity of the segments, since the area of the decimal point is .3 times the area of the average segment.*
4. *Leads of the device immersed to 1/16 inch from the body. Maximum device surface temprature is 140°C.*
5. *For flux removal, Freon TF, Freon TE, Isoproponal or water may be used up to their boiling points.*
6. *All displays are categorized for Luminous Intensity. The Intensity category is marked on each part as a suffix letter to the part number.*

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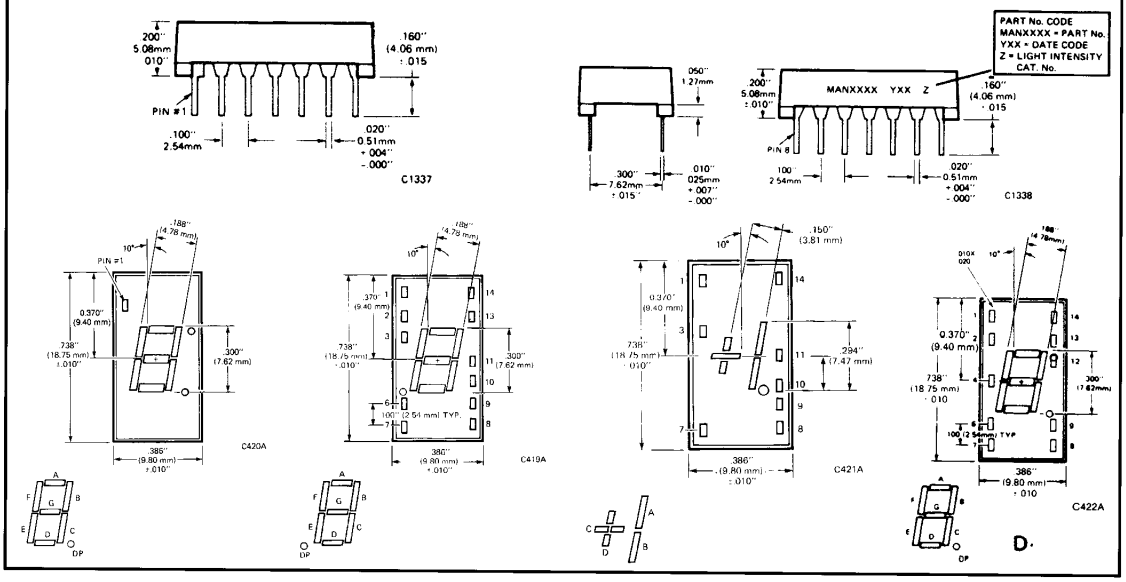
PACKAGE DIMENSIONS



ELECTRICAL CONNECTIONS

Pin No.	ELECTRICAL CONNECTIONS			
	A MAN3410A, 3610A, 71A, 3810A	B MAN3420A, 72A, 3620A, 3820A	C MAN3630A, 73A	D MAN3440A, 3640A, 74A, 3840A
1	Cathode A	Cathode A	Anode C, D	Anode F
2	Cathode F	Cathode F	No Pin	Anode G
3	Common Anode	Common Anode	Anode C, D	No Pin
4	No Pin	No Pin	No Pin	Common Cathode
5	No Pin	No Pin	No Pin	No Pin
6	No Connection	Cathode D.P.	No Pin	Anode E
7	Cathode E	Cathode E	Cathode D	Anode D
8	Cathode D	Cathode D	Cathode C	Anode C
9	Cathode D.P.	No Connection	No Connection	Anode D.P.
10	Cathode C	Cathode C	Cathode B	No Pin
11	Cathode G	Cathode G	Cathode A	No Pin
12	No Pin	No Pin	No Pin	Common Cathode
13	Cathode B	Cathode B	No Pin	Anode B
14	Common Anode	Common Anode	Anode A, B	Anode A

ELECTRICAL SCHEMATIC