

## Basic Logic Gates

### Object

To investigate the properties of the various types of logic gates, and construct some useful combinations of these gates.

### Parts

- (1) 7400 Quad 2-input NAND gate
- (1) 7402 Quad 2-input NOR gate
- (1) 7404 Hex inverter
- (1) 7408 Quad 2-input AND gate
- (1) 7432 Quad 2-input OR gate
- (1) 7486 Quad 2-input XOR gate

### Study sections

*Computer Systems*, Fourth Edition, Jones and Bartlett Publishers: Section 10.1, Boolean Algebra and Logic Gates; Section 10.2, Combinational Analysis.

### General information

The integrated circuit (IC) gates in these labs are of the transistor–transistor logic (TTL) family. TTL logic used to be the most common technology used in the manufacture of computer systems. Because of the lower power requirements and higher density of complementary metal oxide semiconductor (CMOS) technology, however, some form of it is common in today's large scale integrated circuits. TTL gates require +5VDC for a voltage source (VCC) at pin 14 for all ICs in this experiment and ground (GND) at pin 7. The pin numbering system for the ICs is shown in the parts list.

Most integrated circuit chips contain multiple gates. Common configurations are: four gates of 2 inputs each, three gates of 3 inputs each, or two gates of 4 inputs each.

### Caution

Different types of gates (NAND, NOR, etc.) may have their inputs and outputs connected to different pins. Pay close attention during all experiments so that you connect the pins as they are numbered, or the IC may be destroyed. The rule is that you may connect one output to several inputs, but never connect two outputs together. Always turn the power off when connecting or disconnecting wires.

### Procedure

In the following procedure SW stands for switch and is used to set the input level. The switch inputs come from the

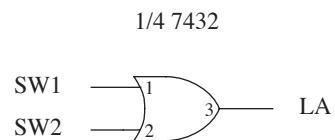
switches on the panel of the breadboard kit. Also, L stands for light, which you implement by connecting an output to one of the light emitting diodes (LEDs) on the panel. As a rule you should make all connections as short as possible except for the switch input leads and the light output leads.

### 1. OR gate function ( $A + B$ )

Install a 7432 Quad 2-input OR gate on the breadboard and make the (VCC) and (GND) connections. Be sure power is off. Make the connections to the gate as shown in Figure 1. The designation 1/4 7432 means that you are using one of the four gates that are provided by the 7432 chip. The small numbers inside the gate are the pin numbers from the chip package. Turn on the power. Set the switches as indicated in the truth table of Figure 1 and record the light conditions (on = 1), (off = 0).

**Figure 1**

SW1	SW2	LA
0	0	
0	1	
1	0	
1	1	

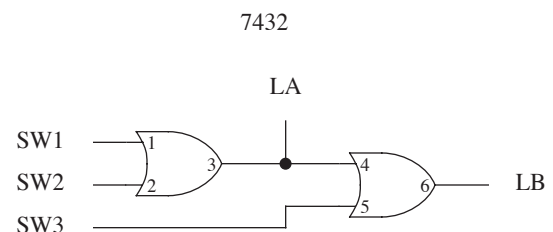


### 2. Two-level 3-input OR gate

Make the connections as shown in Figure 2. Set the switches as shown in the truth table of Figure 2 and record the light conditions.

**Figure 2**

SW1	SW2	SW3	LA	LB
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

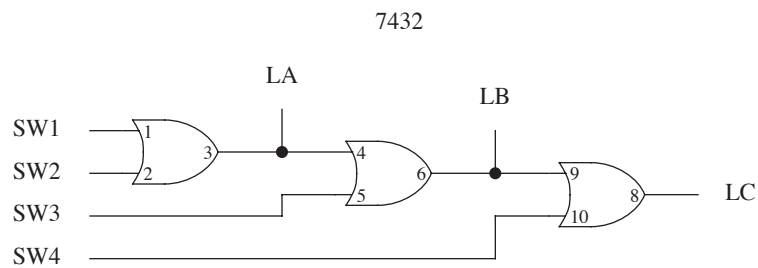


### 3. Three-level 4-input OR gate

Wire the circuit shown in Figure 3. Set switches as indicated in the truth table of Figure 3 and record the light conditions.

**Figure 3**

SW1	SW2	SW3	SW4	LA	LB	LC
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

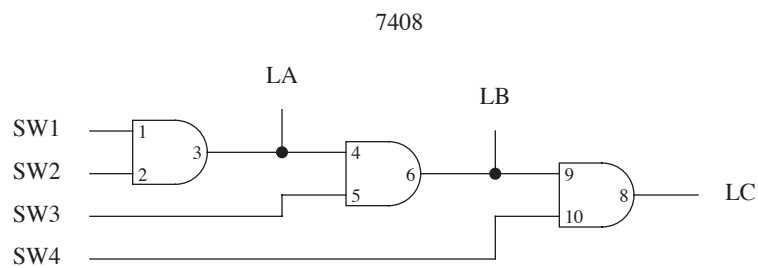


#### 4. AND gate function (AB)

Turn off the power and remove the 7432 OR gate. Without changing the wiring replace with a 7408 Quad 2 input AND gate. The schematic representation of the three level 2 input AND gate is shown in Figure 4. Set the switches as indicated in the truth table of Figure 4 and record the light conditions.

**Figure 4**

SW1	SW2	SW3	SW4	LA	LB	LC
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			



Propagation delay is the time between application of a change to the input and the appearance of the resulting change on the output. While the time is insignificant in human terms (on the order of 10-15 nanoseconds for TTL technology), it often becomes critical in high speed circuits. The above circuit contains three propagation delays, hence the name three-level circuit. However, it may be reduced to a two level circuit using the same number of gates.

Draw the equivalent two-level 4-input circuit using three 2-input AND gates in the space below. Only the output (LC) column of the truth table need be satisfied. You do not need to construct the circuit in the lab.

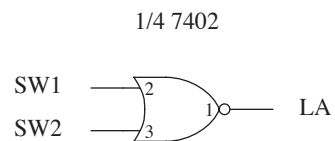
Equivalent 2-level circuit:

### 5. NOR gate function $(A + B)'$

Install a 7402 Quad 2-input NOR gate as shown in Figure 5. Set the switches as indicated in the truth table of Figure 5 and record the light indications. Note that the truth table is identical but reversed to that of the OR gate. Thus the NOR gate is identical to an OR gate followed by an inverter.

**Figure 5**

SW1	SW2	LA
0	0	
0	1	
1	0	
1	1	

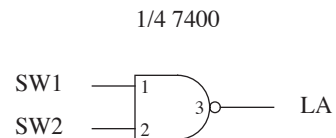


### 6. NAND gate function $(AB)'$

Turn off the power and remove the 7402 NOR gate. Install a 7400 Quad 2-input NAND gate and connect as shown in Figure 6. Set the switches as indicated in the truth table of Figure 6 and record the light conditions. Note that the NAND function is to the AND as the NOR is to the OR.

**Figure 6**

SW1	SW2	LA
0	0	
0	1	
1	0	
1	1	

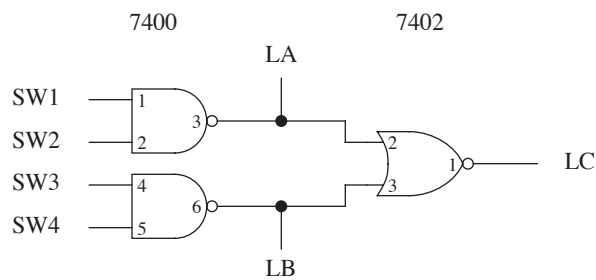


### 7. The negated-input OR and the negated-input AND concept

Connect the circuit shown in Figure 7. Set the switches as indicated in the truth table of Figure 7 and record the light indications. Compare the truth table of Figure 7 with that of the 4-input AND gate of Figure 4. Note that the output columns (LC) are identical. Therefore the circuit of Figure 7 is performing the 4-input AND function, although the second level gate is a NOR gate.

**Figure 7**

SW1	SW2	SW3	SW4	LA	LB	LC
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			



Inspection of the circuit in Figure 7 is misleading as to its actual function, due to the NOR symbol, especially if it were part of a complex logic diagram which was being analyzed. Therefore, it has become conventional to draw the negated input AND function of the NOR gate as in Figure 8.

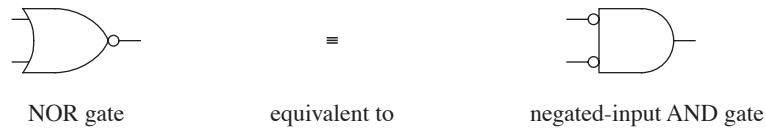
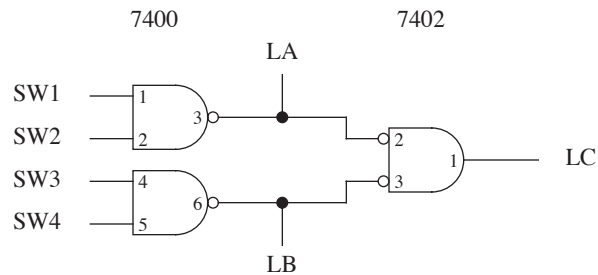
**Figure 8**

Figure 9 shows the equivalent circuit of Figure 7, redrawn so that its function becomes readily apparent. In your mind you can simply cancel the effect of two inverters in a row.

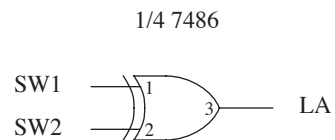
**Figure 9**

## 8. The XOR function

Connect the circuit shown in Figure 10. Set the switches as shown in the truth table of Figure 10 and record the light indications.

**Figure 10**

SW1	SW2	LA
0	0	
0	1	
1	0	
1	1	



It can be seen from the truth table that the XOR gate is similar to the OR gate with the exception of the state in which both inputs are high. This feature makes the gate useful for binary adders, parity generators, etc.

You have now illustrated the function of each type of gate in actual operation, except for the inverter. As the inverter simply changes the input signal to the opposite level (1 to 0, 0 to 1) we will illustrate it only by its function as we use



it in the next setups.

Normally there is a large preponderance of NAND and NOR gates in a logic design, with few or no AND and OR gates. As we have seen, the NAND and NOR gates invert the signal, and this low assertion is useful in a great number of instances. For example, the NAND and NOR gates may be used as inverters by applying the input signal to all of the inputs of the gate, or by tying unused NAND inputs to VCC and unused NOR inputs to GND. Thus we may invert the outputs of the NAND and NOR gates by adding another gate as an inverter so as to obtain the AND and OR functions. However, as the AND and OR gates do not invert, it is not possible to derive the NAND and NOR functions from them.

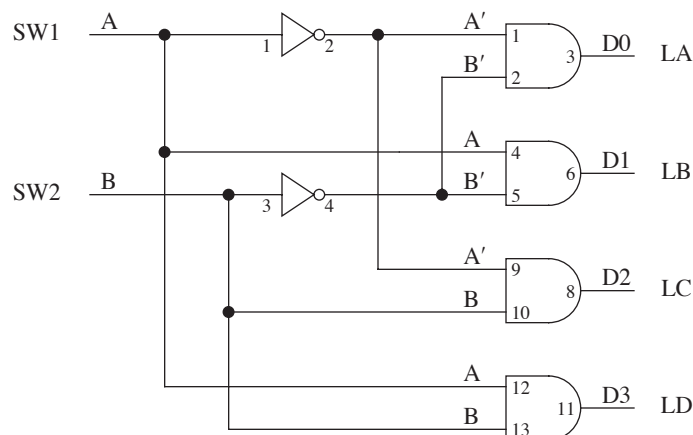
### 9. A mystery circuit

Connect the circuit of Figure 11. Set the switches as shown in the truth table of Figure 11. Set the switches as shown in the truth table of Figure 11 and record the light indications. If the inputs are considered as a two-bit binary word, with A being the least significant bit (LSB) and B being the most significant bit (MSB), what is the name of this circuit?

Name of circuit: \_\_\_\_\_

**Figure 11**

B SW2	A SW1	D0 LA	D1 LB	D2 LC	D3 LD
0	0				
0	1				
1	0				
1	1				



Redesign the circuit to operate in exactly the same manner if the only components available were six 7402 NOR gates. Use two gates as inverters and draw the other four as negated-input AND gates. Show the circuit diagram below but do not construct the circuit in the lab.

Equivalent circuit with only six 7402 NOR gates: