A Combined Combinational-Sequential System

Object

To construct a serial transmission circuit with a comparator to check the output.

Parts

(2) 7485 4-bit magnitude comparators

(1) 74177 4-bit binary counter

(1) 74151 8-line to 1-line data selector/multiplexer

(1) 74164 8-bit parallel output shift register

Study sections

Computer Systems, Fourth Edition, Jones and Bartlett Publishers: Section 10.4, Combinational Devices; Section 11.1, Latches and Clocked Flip-Flops, 11.3 Computer Subsystems.

General information

Combinational and sequential logic circuits each have their place in digital systems and subsystems. More often, the sequential circuit is used for temporarily storing control or data information which is being, or will be, used by a combinational circuit to test, compare, or perform arithmetic operations. In this experiment you will construct a small system which will change parallel information to serial information, transmit it through a single data line in serial format, reassemble the data to parallel form and compare the reassembled word to the original word for errors.

In previous experiments you have constructed various logic devices using logic gates and flip-flops. As logic design grew larger and more complex, the needs for simplification of interconnections generated a new series of integrated circuits, known as MSI (Medium Scale Integration), which has many internal interconnections. The simpler gate and flip-flop IC's then were called SSI (Small Scale Integration). Still more complex IC's have been named LSI (Large Scale Integration). The circuit that you will construct in this lab uses MSI IC's in the type of connection that might be found as a transfer circuit between a computer and a peripheral device.

Description

The 74177 binary counter in the transmitting section of the circuit acts as the main controlling device. It is a divide-by-sixteen counter which is in two sections: divide-by-two, and divide-by-eight. As we are only concerned with the eight bits of information, you will use only the divide-by-eight section. When the counter has been reset, the three output lines (one from each stage) will be at 000. With the application of clock pulses the output lines will sequentially present binary numbers up through 111.

The 74151 multiplexer is a combinational circuit containing gates arranged in such a way that each three-bit binary number presented at the control inputs will connect the input bit association with that number to the output. Thus a sequential count from 000 to 111 will cause the out put to "read" the eight input lines, and place them on the output one after another, or serially.

At the other end of the transmission line, the same clock that steps the counter, clocks the bit presented on the line into the register. After all eight bits have been clocked into the register, the parallel register outputs will hold the eight-bit word as multiplexer inputs.

To verify that the received eight-bit words is identical to the original word, a pair of 7485 4-bit magnitude comparators are used. These combinational circuits, in addition to the inputs for the words being compared, have three additional inputs and three outputs. The outputs indicate whether word A is greater, smaller, or equal in value to word B. The three inputs permit cascading the comparators, as is done in this implementation. Note that the inputs of the first comparator are variously tied low and high. These connections simulate an output from a previous comparator that indicates equality, thus setting up the first comparator to make its own decision. These comparators would not normally be used in a transmission system. They are in this circuit so you may verify its proper operation.

The timing of the data transfers is important in this circuit. When the 74177 counter is reset, and the B, C, and D outputs are all zero, the zero-bit of the data inputs is on the output line. This bit must be clocked into the shift register before the clock changes the counter inputs 001. This is possible because the shift register is clocked on the rising, or leading edge of the clock pulse, while the counter is clocked on the falling, or trailing edge of the clock pulse. Thus the data on the transmission line is always clocked into the shift register before the counter is stepped to the next data bit. If both IC's required the same edge, we would have to invert the clock pulse to the counter to obtain the same result.

Procedure

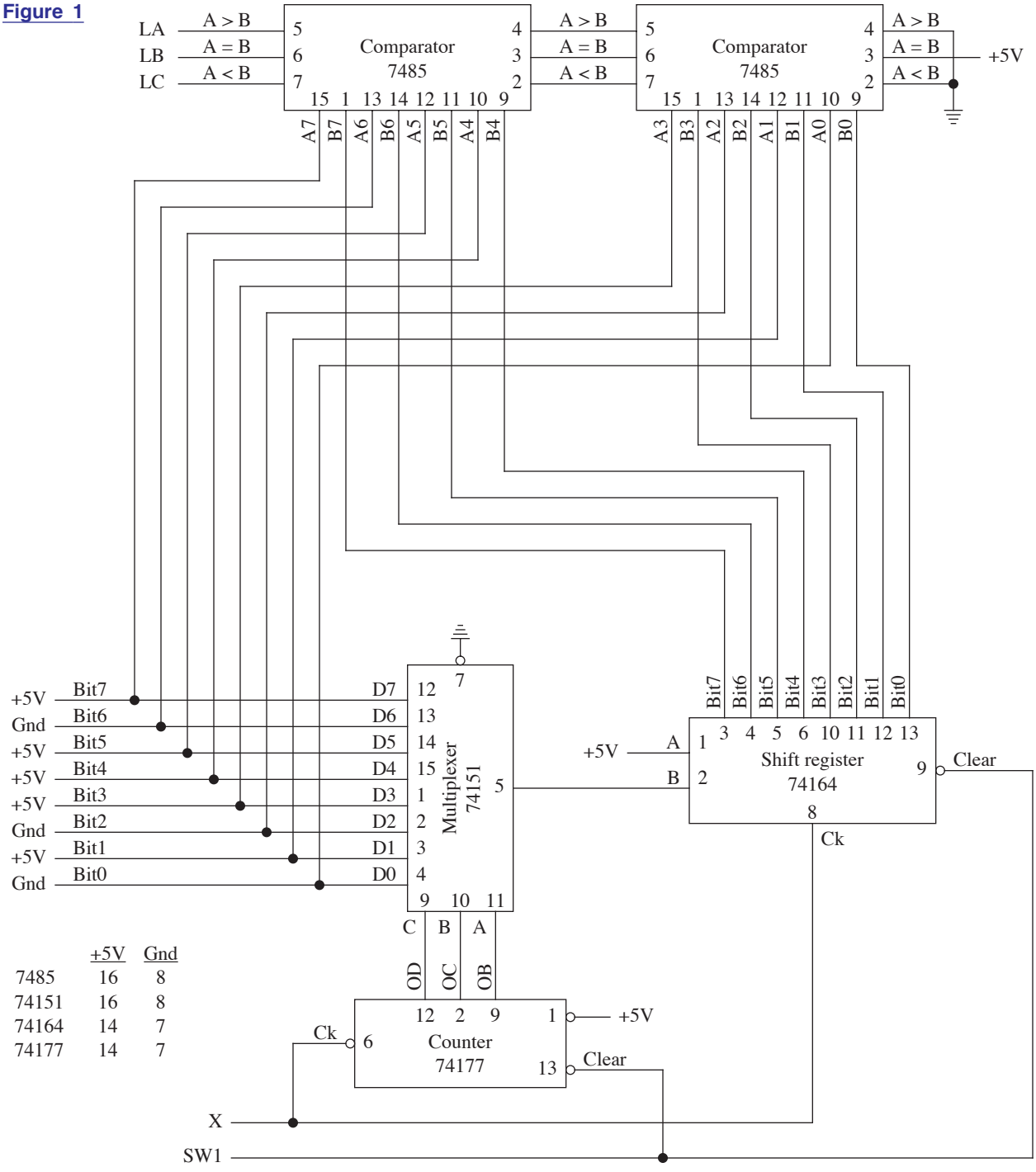
Wire the circuit as shown in the logic diagram, Figure 1. Connect the data input lines to +5V and ground as indicated. SW1 is normally on. X is normally off.

Set Sw1 off then on to reset the circuit. LA should be lit.

Clock X eight times. After the eighth clock pulse, LB should come on. This indicates a successful data transfer. During the transfer process, either LA or LC will be lit. If the proper indication does not occur, check for miswires in the circuit.

After verifying that the circuit works properly, set SW1 off then on to reset the circuit. Complete the timing diagram of Figure 2 by clocking X and checking the indicated points for a high or low condition after each step. Note: Levels may change on the leading or trailing edge of the clock. Record it accordingly!

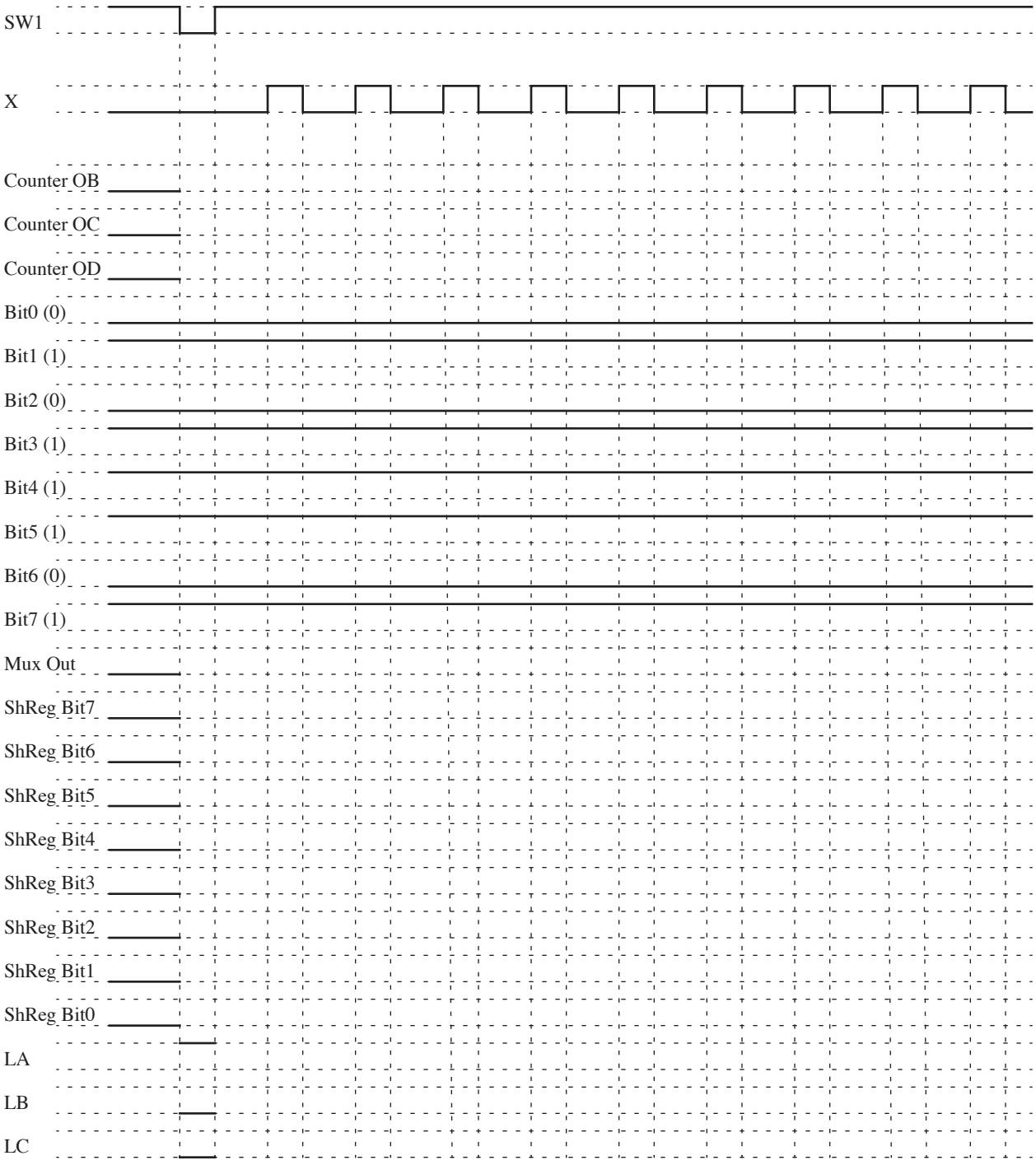
Figure 1



	+5V	Gnd
7485	16	8
74151	16	8
74164	14	7
74177	14	7

Instructor verification: _____

Figure 2


SW1
X
Counter OB
Counter OC
Counter OD
Bit0 (0)
Bit1 (1)
Bit2 (0)
Bit3 (1)
Bit4 (1)
Bit5 (1)
Bit6 (0)
Bit7 (1)
Mux Out
ShReg Bit7
ShReg Bit6
ShReg Bit5
ShReg Bit4
ShReg Bit3
ShReg Bit2
ShReg Bit1
ShReg Bit0
LA
LB
LC

Questions

1. Describe what might occur if both the counter and the shift register required the same pulse edge for clocking.

2. Referring to the data sheet, what is the function of pin 7 of the 74151? What would happen in the experiment if the pin were set to a high condition?

3. What is the function of pin 1 of the 74177? What pins would the input come from if pin 1 were grounded? What would happen in this experiment if pin 1 were grounded?

4. What is the function of pin 1 of the 74164? What would happen in the experiment if this pin were grounded?

5. Why are three connections between the comparators needed? When does the first comparator need the input from the second comparator?

6. Why is pin 3 of the second comparator tied to +5V?

7. If the counter were not reset initially, LB would not come on after the eighth clock pulse. Explain whether LB would or would not come on with more clock pulses.

NOTE: This lab illustrates serial transmission between the multiplexer and shift register. Questions 8 and 9 are given with the assumptions that the direct connection between the input and comparitors are not in the circuit and that the magnitude comparators are also not in the circuit. They would not normally be used, and are given only for the purpose of verifying that the transmission occurred correctly.

8. What is the main advantage of using this circuit to transmit data over a long distance rather than connecting the data lines directly?

9. What is the main disadvantage?

10. Without the direct connection between the inut and the comparitors, is there a way to check if the transmission is correct? _____ If so, how?